

CMOS High-Speed I/O

- Background, Circuits, and Future Trends -

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Nov. 26th, 2004

Outline

◆ Background

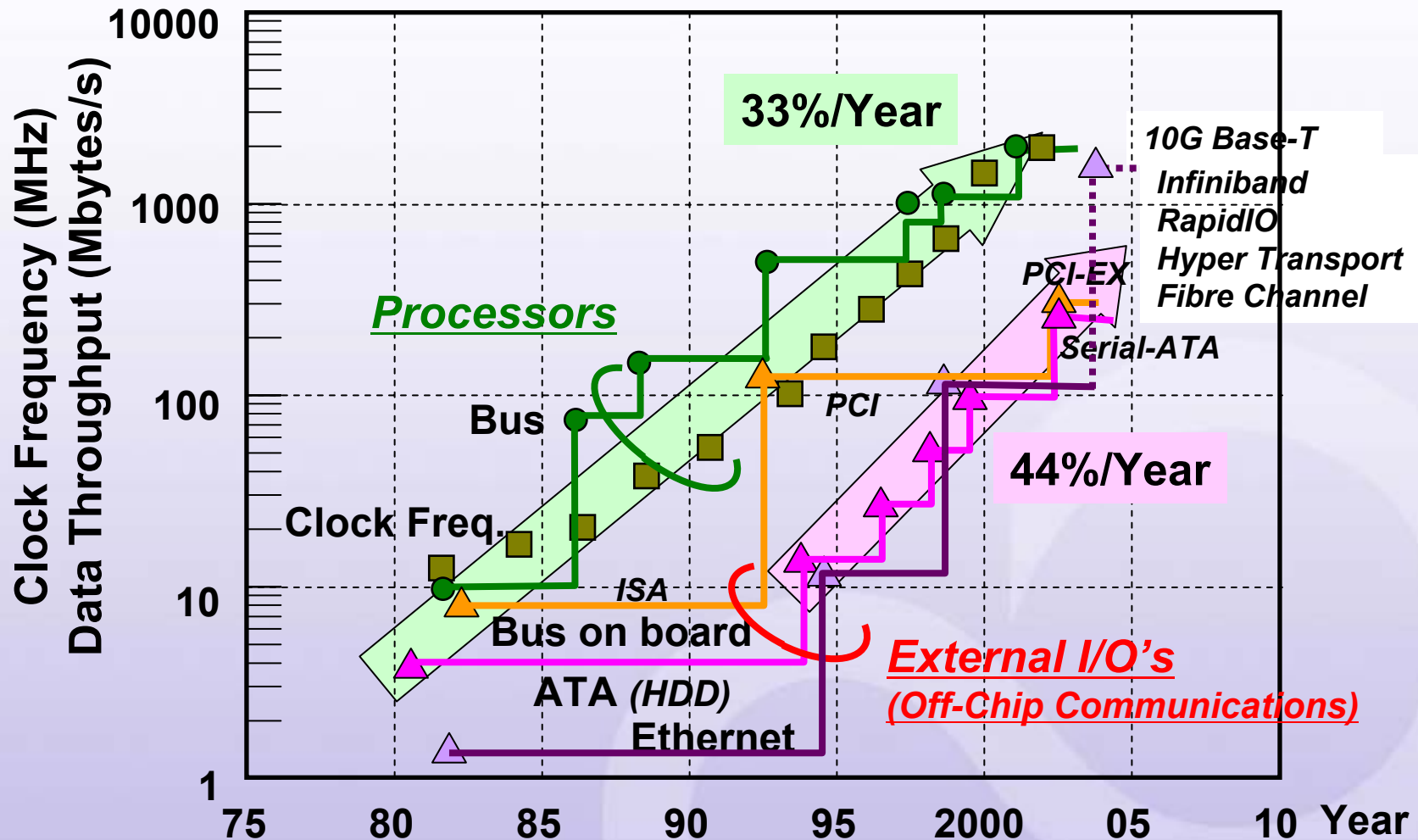
- ◆ Trends in IC bandwidth
- ◆ Pin-bandwidth bottleneck

◆ Circuit solutions for bandwidth bottleneck

- ◆ Multi-bit, multi-port I/O applications
- ◆ Clock recovery scheme
- ◆ Receiver and transmitter front ends

◆ High-speed-I/O Future trends

On-chip/off-chip data rate trends



Growth Rates of Performance and BW

- ◆ **C: Performance, N: Number of grids, f: frequency**

$$\underbrace{C}_{1.68/\text{year}} \equiv \underbrace{N}_{1.26/\text{year}} \times \underbrace{f}_{1.33/\text{year}}$$

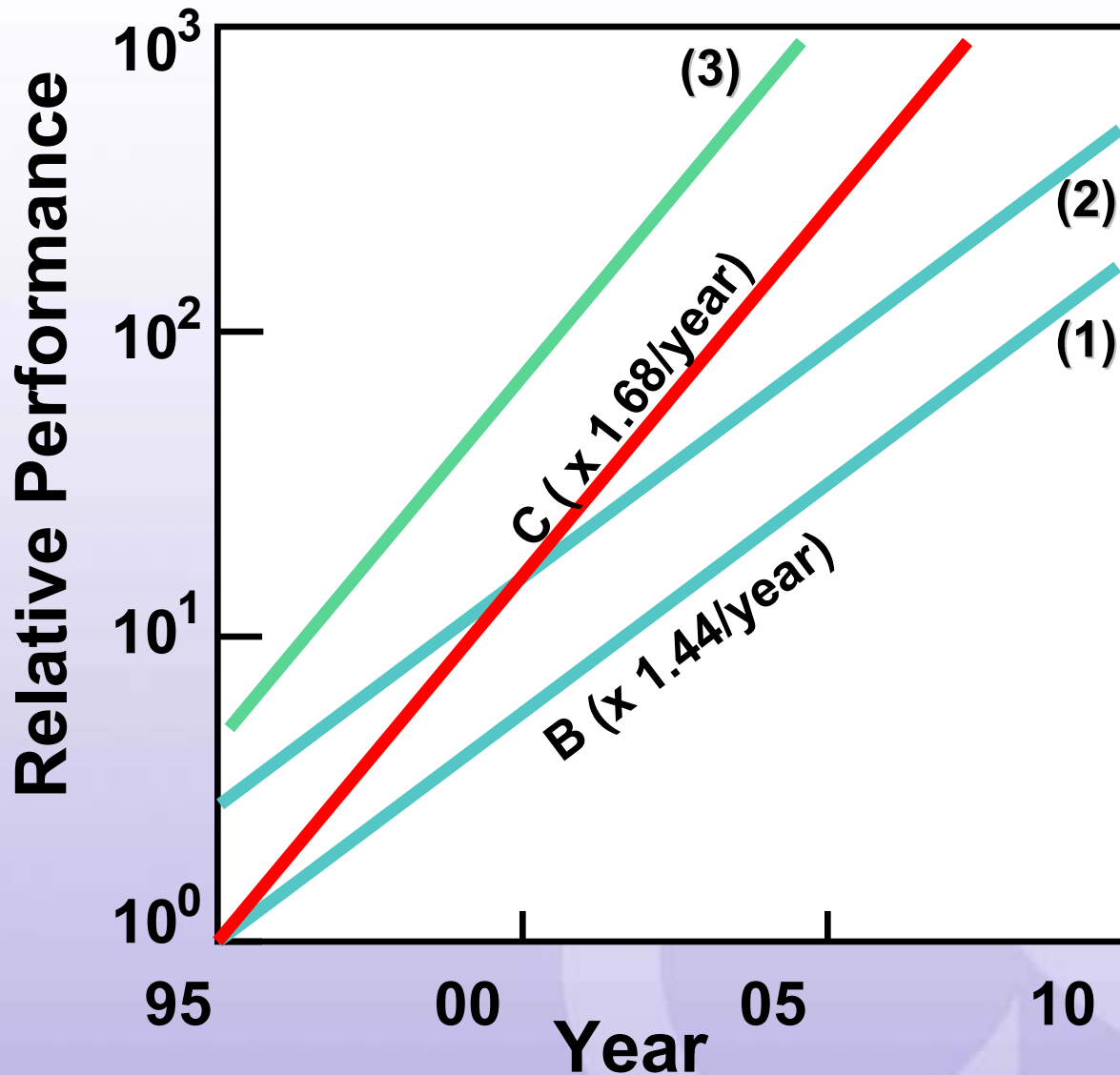
- ◆ **B: bandwidth needed for the performance**

$$\underbrace{B}_{1.44/\text{year}} = kC^\alpha \quad \alpha \approx 0.7 \quad (\text{typical}) \quad \text{(Rent's law)}$$

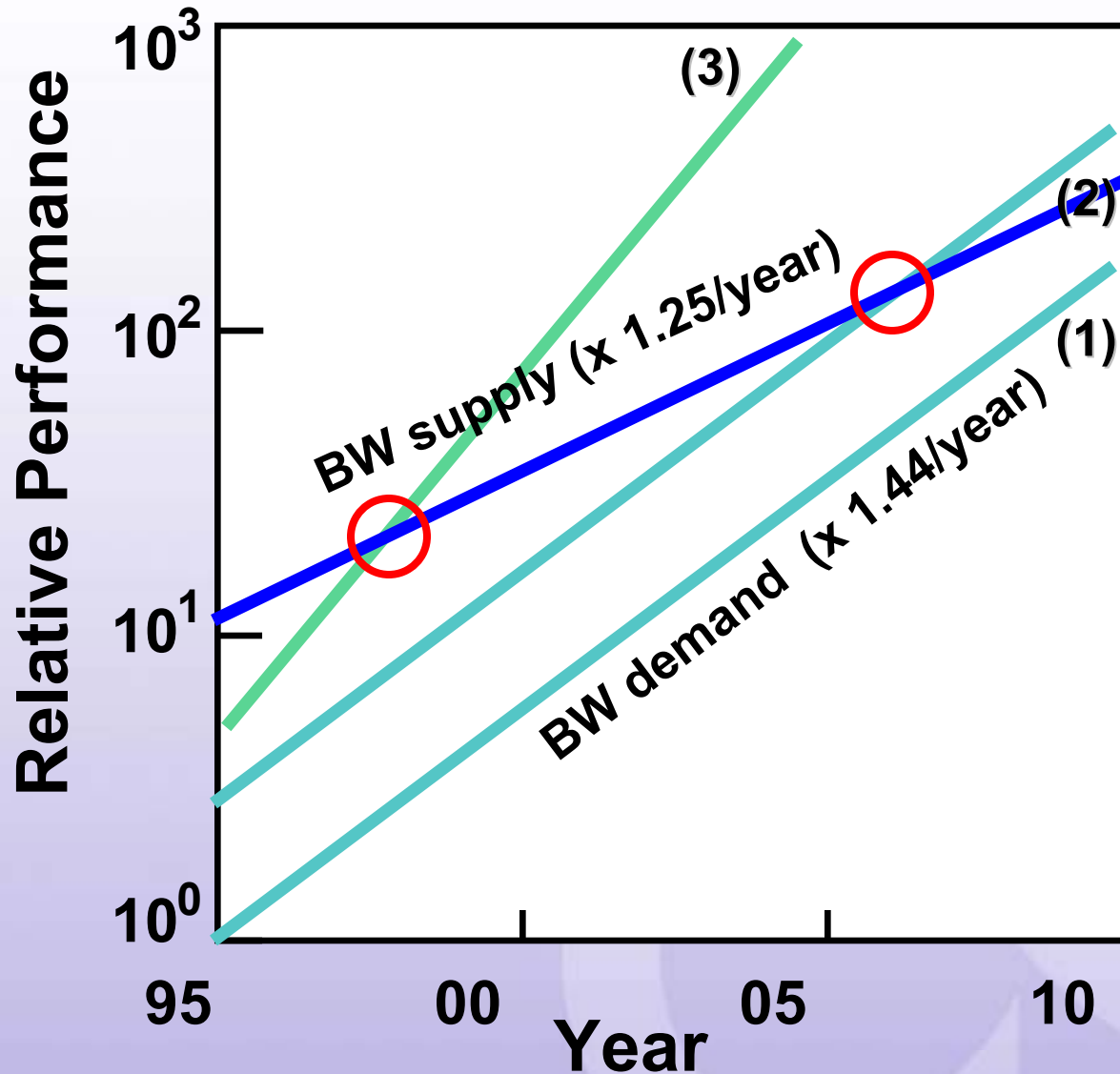
- ◆ **B_{chip}: Maximum obtainable bandwidth**

$$\underbrace{B_{chip}}_{1.25/\text{year}} = \underbrace{B_{pin}}_{1.20/\text{year}} \times \underbrace{N_{pin}}_{1.04/\text{year}}$$

Trend in BW Demands



BW Supply and Demand Gap



Implication of Pin-Bandwidth Bottleneck

◆ Before bottleneck

- ◆ Pin BW is not the primary concern
- ◆ Data rate per pin does not have to be maximized

◆ After bottleneck

- ◆ Pin BW can be the most significant bottleneck
 - ◆ Both the pin data rate and the number of pin should be maximized
 - ◆ Need continuous improvement in circuit topology

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- ◆ Trends in IC bandwidth
- ◆ Pin-bandwidth bottleneck

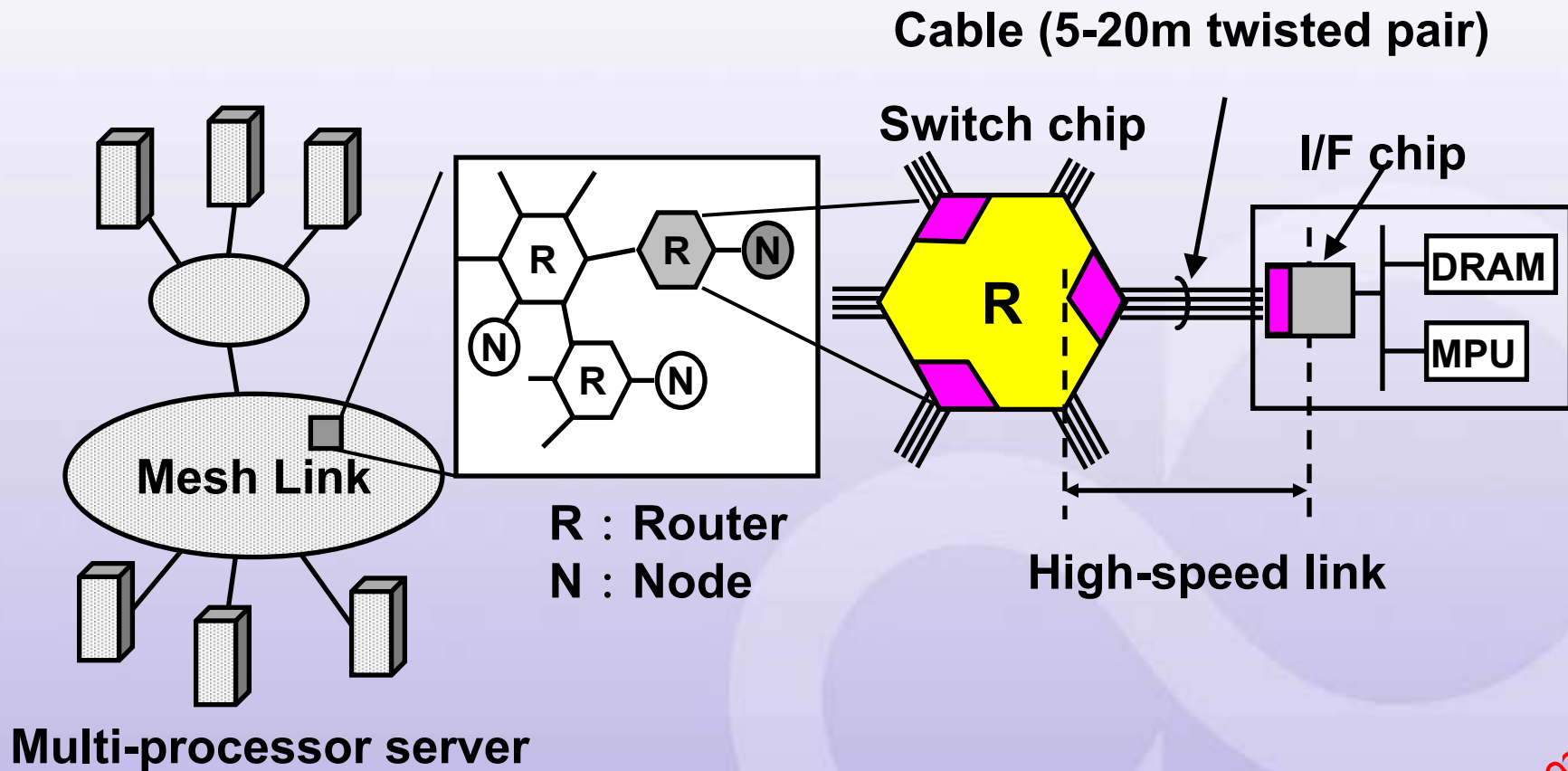
◆ Circuit solutions for bandwidth bottleneck

- ◆ Multi-Gigabit, Multi-bit I/O applications
- ◆ Clock recovery scheme
- ◆ Receiver and transmitter front ends

◆ High-speed-I/O Future trends

HSIO Application (@late 90's)

- ◆ High-speed link for server and storage
- ◆ 2.5GByte/s/direction (1.25Gb/s x 2 Byte x2)



Issues (@late 90's)

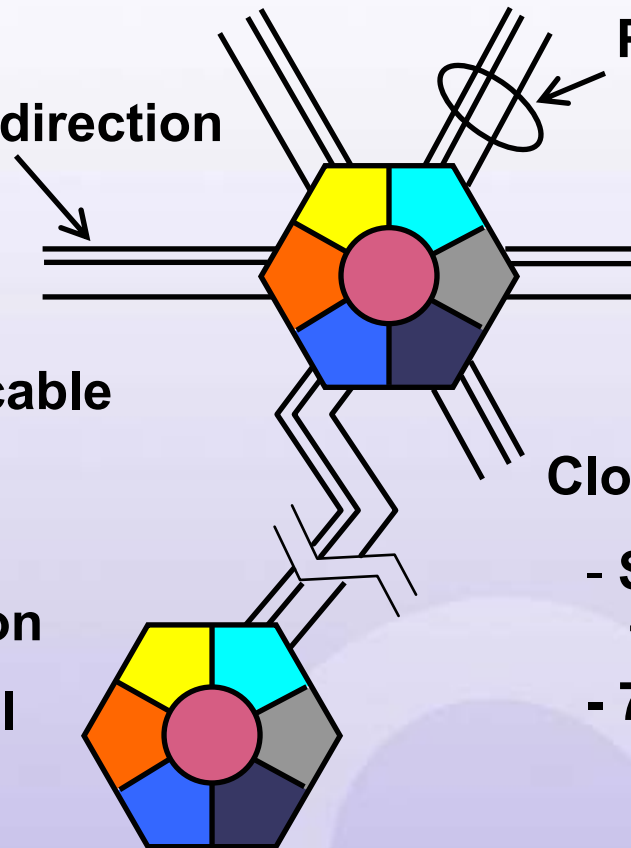
◆ Multi-Gb/s, multi-bit, multi-port link

High data rate

- 1.25 Gbps/signal/direction

Use both PCB and cable

- 1.25 Gbps@5m
- 625 Mbps@20m
- Needs equalization
- Amplitude control



Parallel link

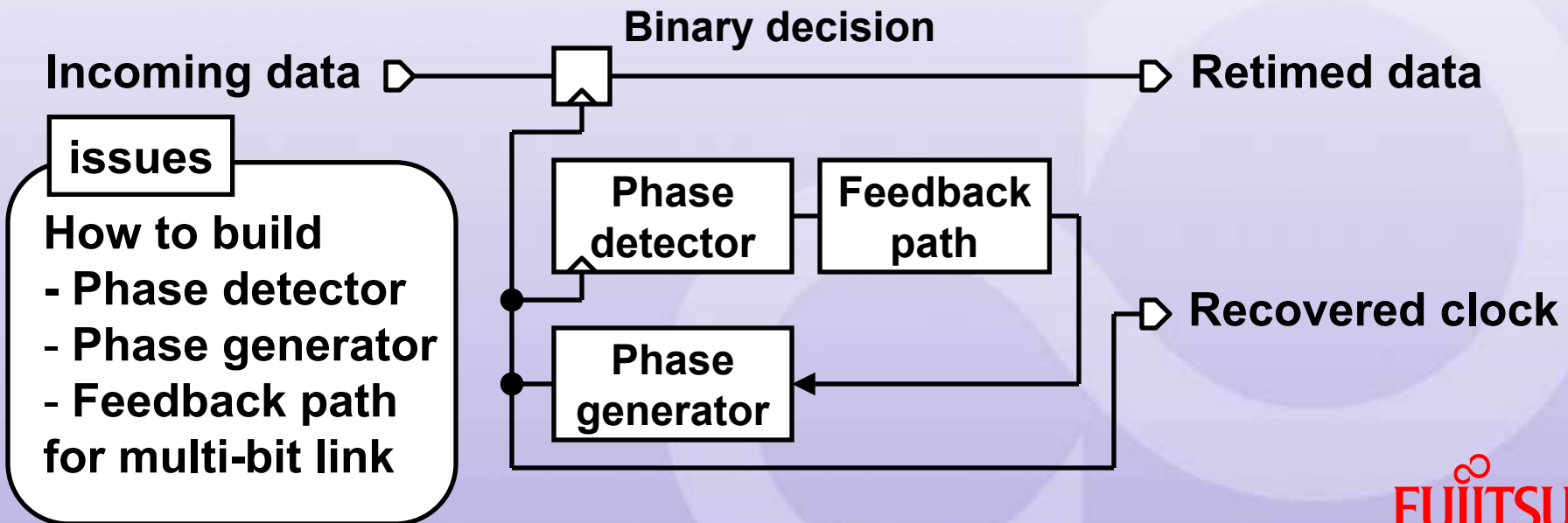
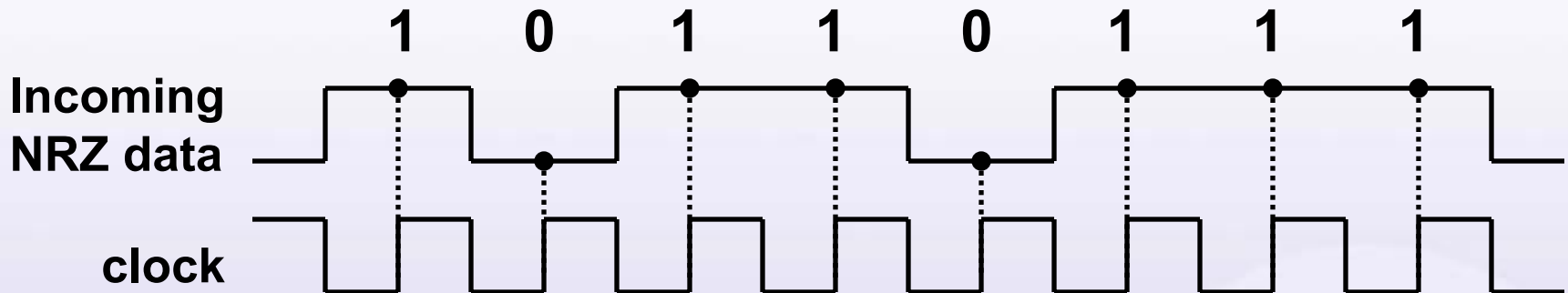
- Need per-bit de-skew
- Many transceivers (126TRX/chip)

Clocking

- Should allow 100-ppm frequency deviation
- 7 clock domains

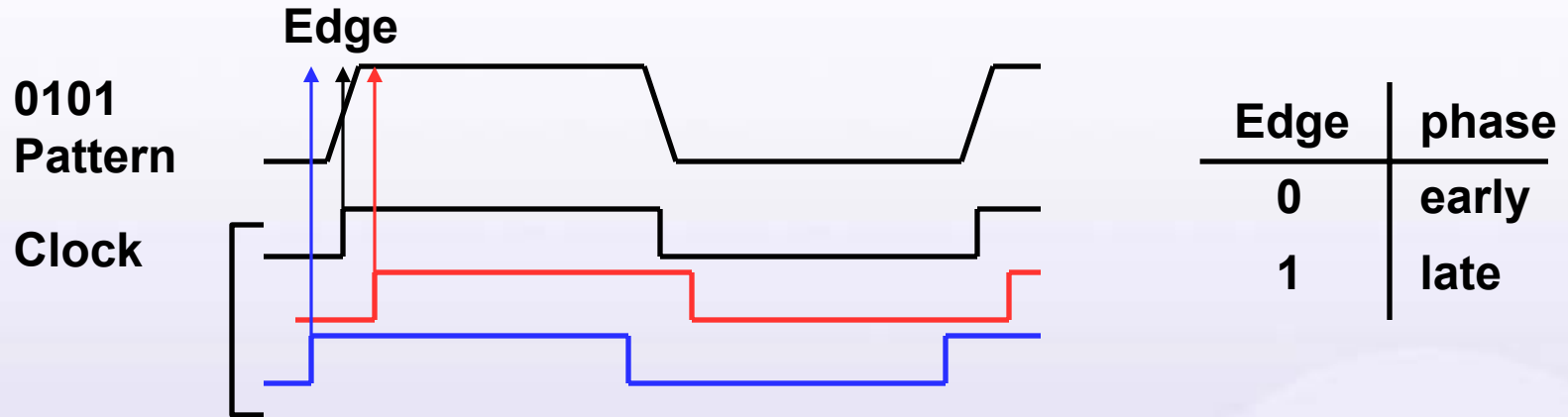
Clock Recovery

- ◆ Means to track the input phase needed
 - ◆ Use feedback from phase detector to phase generator

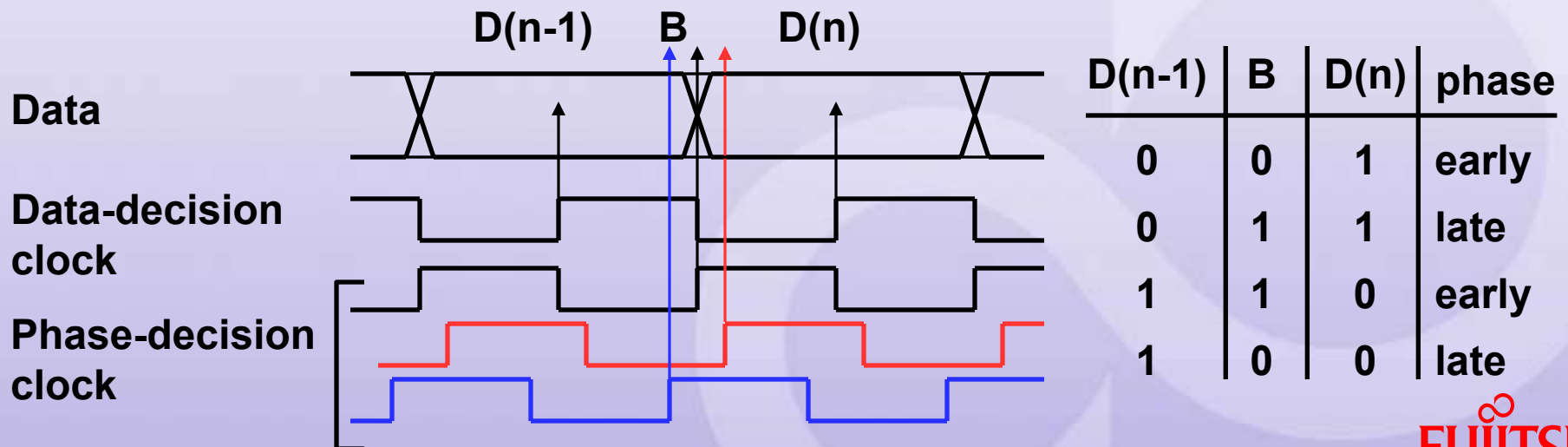


Bang-bang Phase Detection

◆ Clock-phase extraction from 0101 pattern



◆ Phase extraction from data



Linear or Bang-bang?

◆ Linear detector

- ◆ Well-defined Gain and loop behavior
- ◆ May have systematic phase error

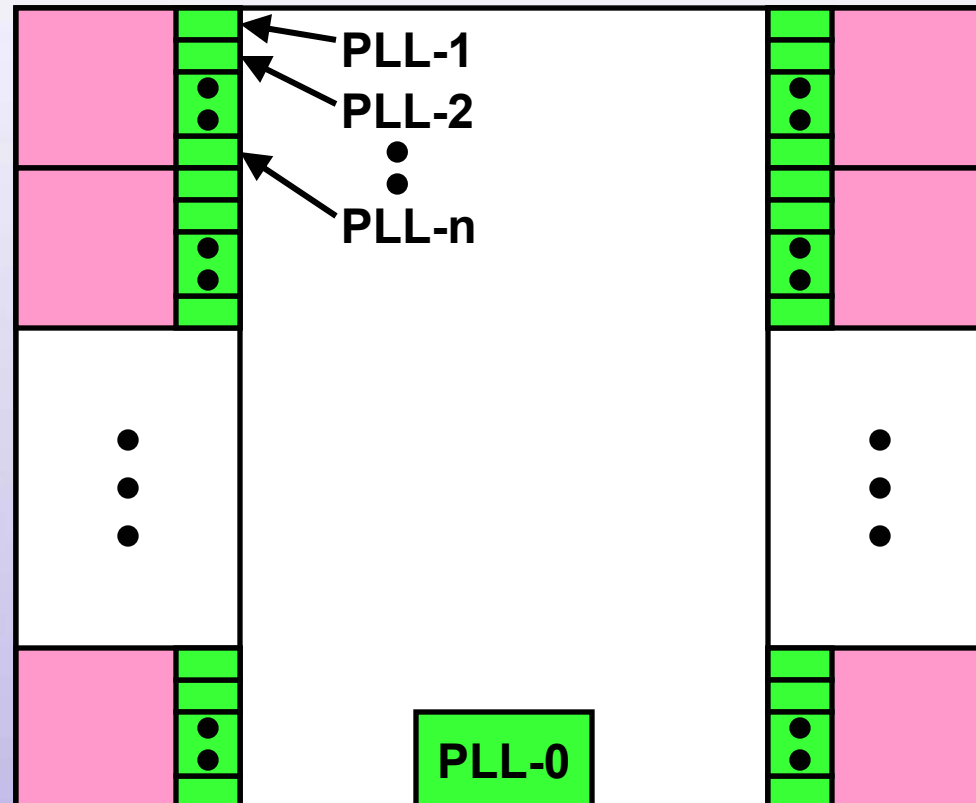
◆ Bang-bang detector

- ◆ Can use the same decision circuit for both the data decision and phase detection
 - ◆ No systematic phase error
- ◆ Output compatible with logic circuit

◆ We chose bang-bang detector for our link

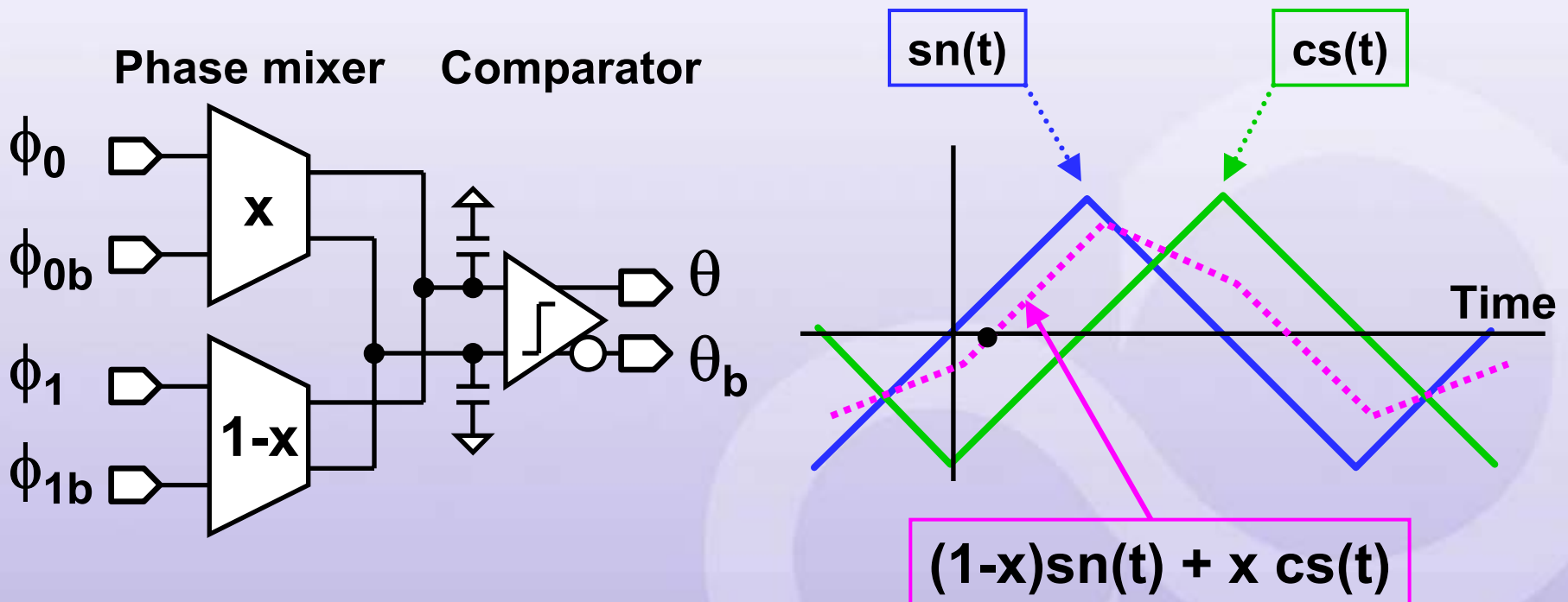
Clock Recovery for Multiple Clock Domains

- ◆ Can we place many PLLs on a single chip?
 - ◆ VCOs run with different frequencies ($\Delta f \sim 100\text{ppm}$)
 - ◆ Concern: interaction through injection locking



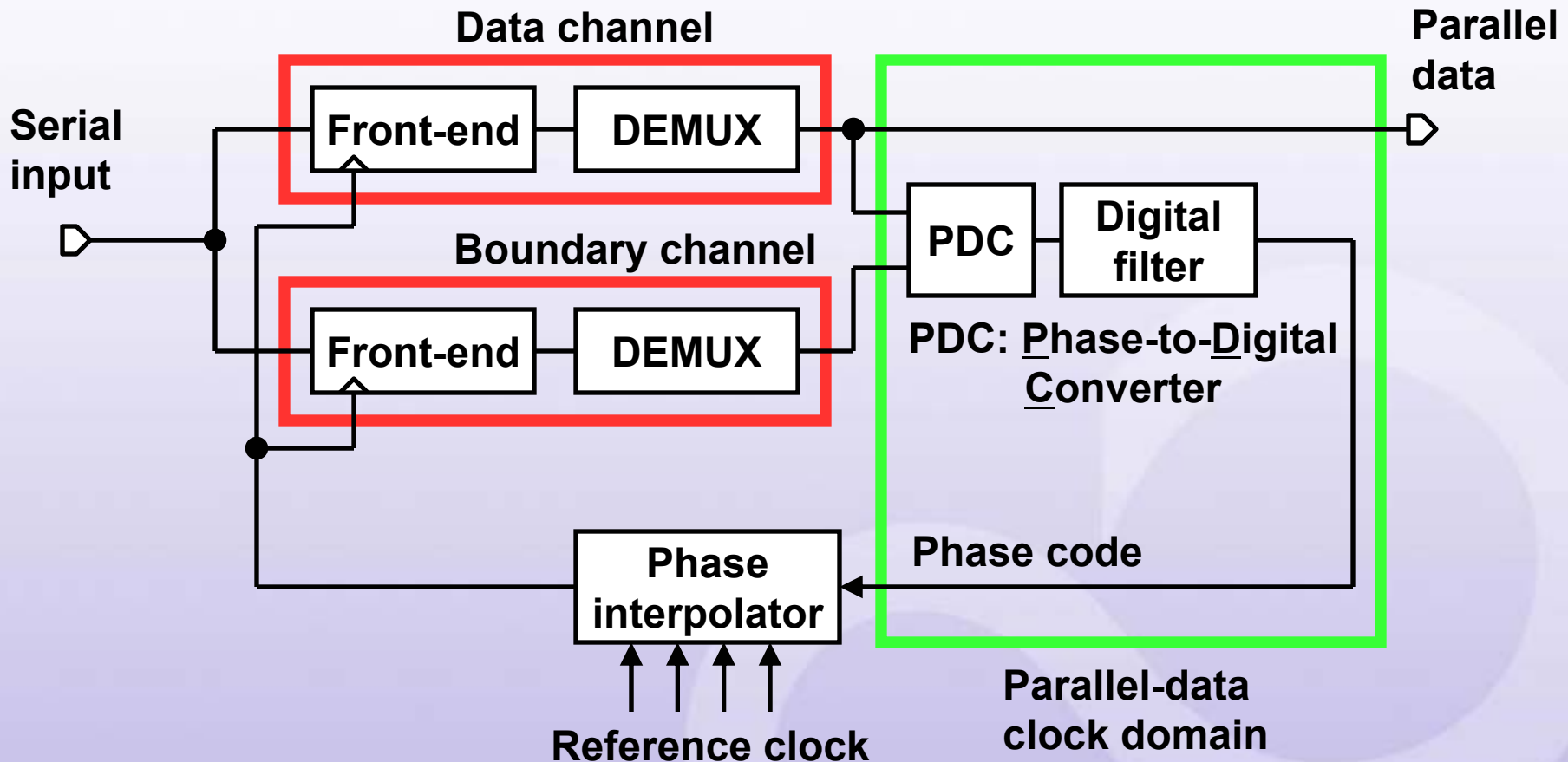
Phase Generation by interpolation

- ◆ Generate phase by weighted sum of reference clocks
 - ◆ No oscillator, thus no injection locking
- ◆ Weights are controlled by DACs
 - ◆ Works as a digital-to-phase converter



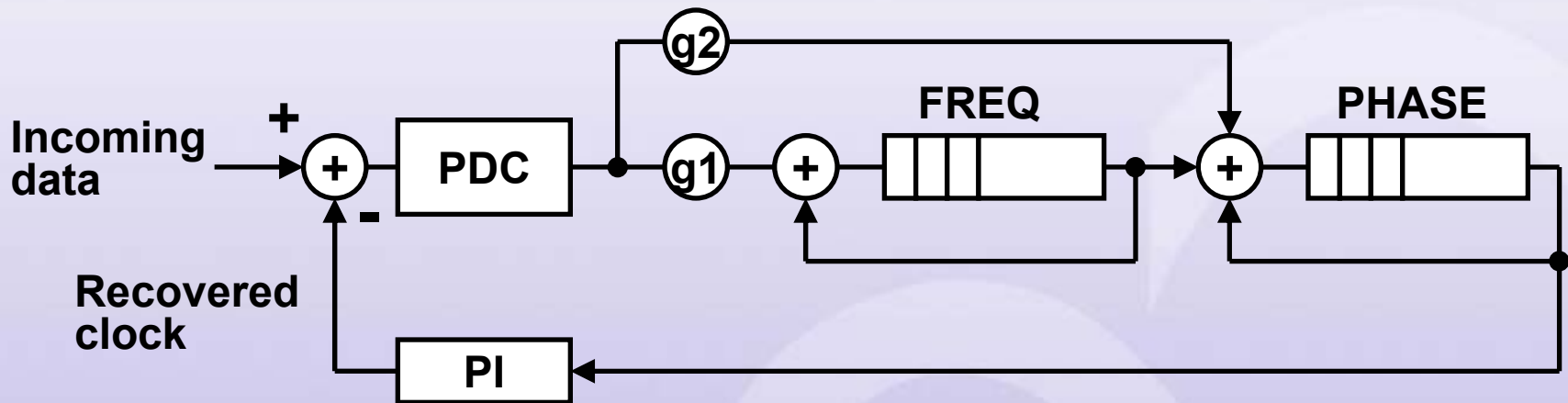
Phase-control Feedback Loop

- ◆ Feedback path is composed of logic circuits in parallel-data clock domain



Second-order Feedback Loop

- ◆ Two registers that store frequency and phase errors
 - ◆ No tracking error for static frequency difference
 - ◆ Equivalent to second-order PLL



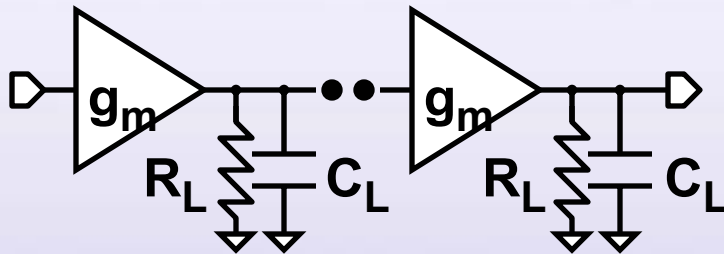
Front-end Comparator

◆ Amplifier or regenerative latch

- ◆ Regenerative latch is faster for a given technology

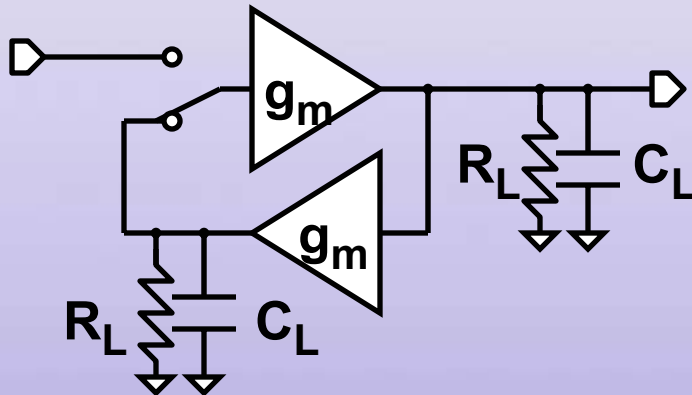
$$A \equiv g_m R_L, \tau \equiv R_L C_L, \tau_0 = C_L / g_m$$

n-stage amplifier



$$\tau \cong n R_L C_L = n A \tau_0$$

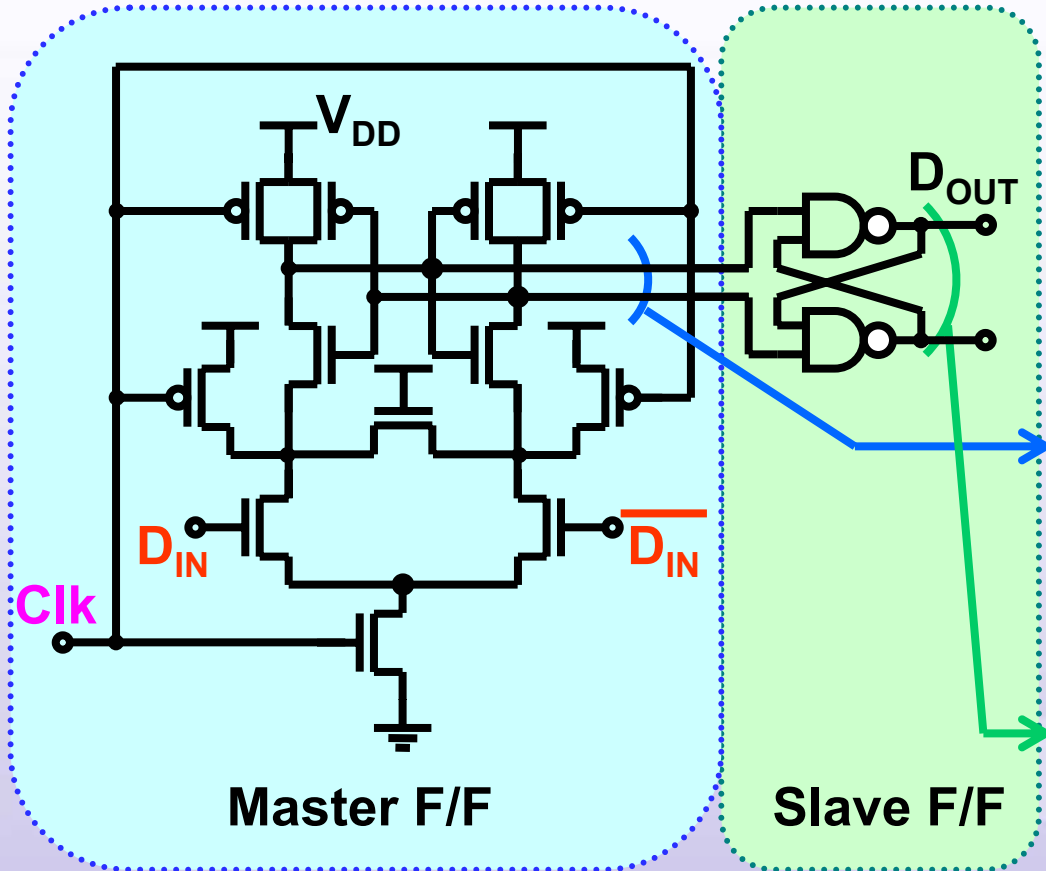
Regenerative latch



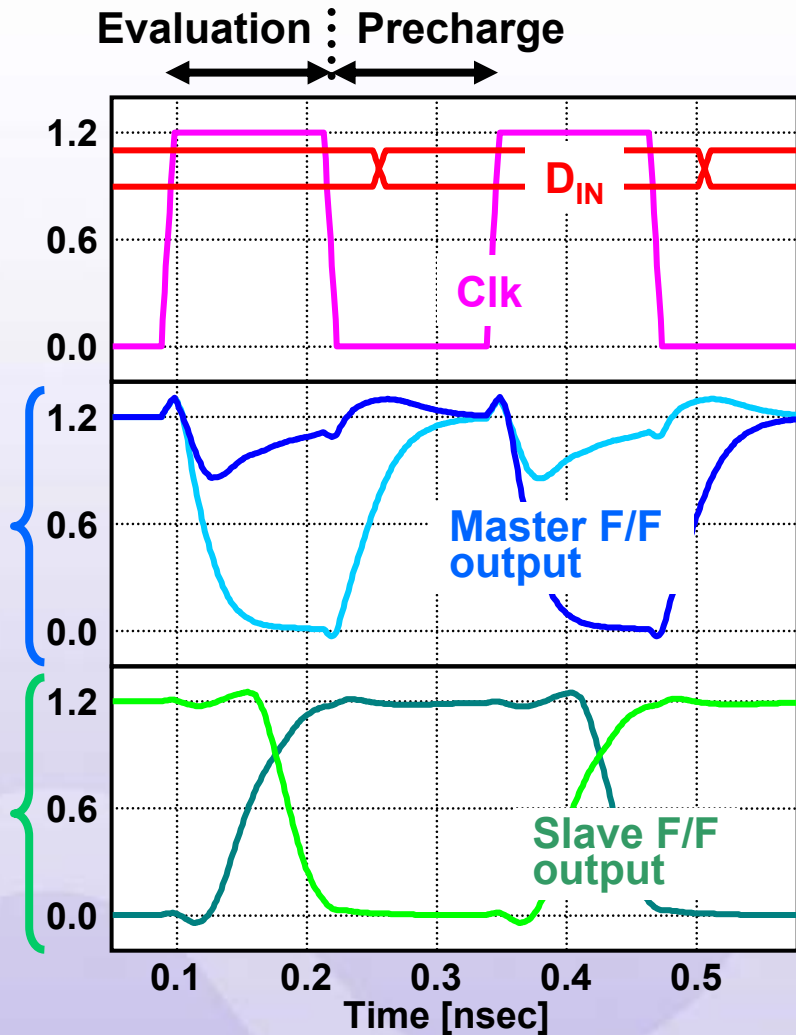
$$\Delta V = \Delta V_0 \exp[(A - 1)t / \tau]$$

$$\tau_{latch} = \frac{\tau}{A - 1} \cong \frac{\tau}{A} = \tau_0$$

Strong-Arm-Type Decision F/F Circuit



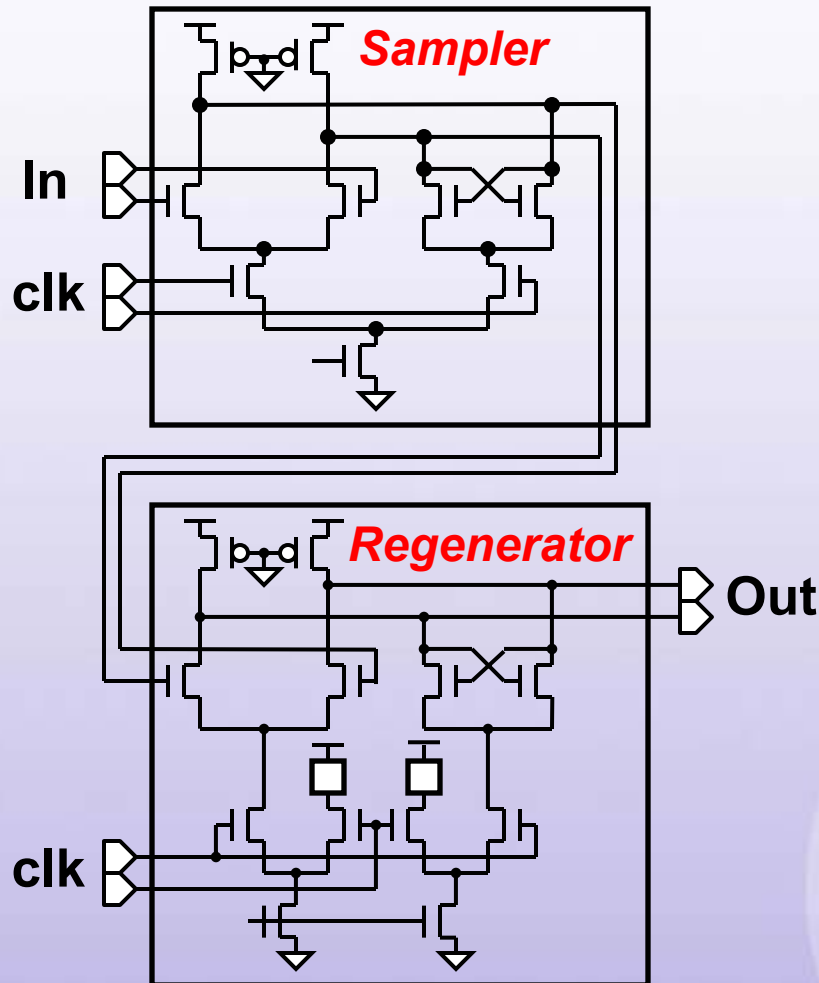
Schematic



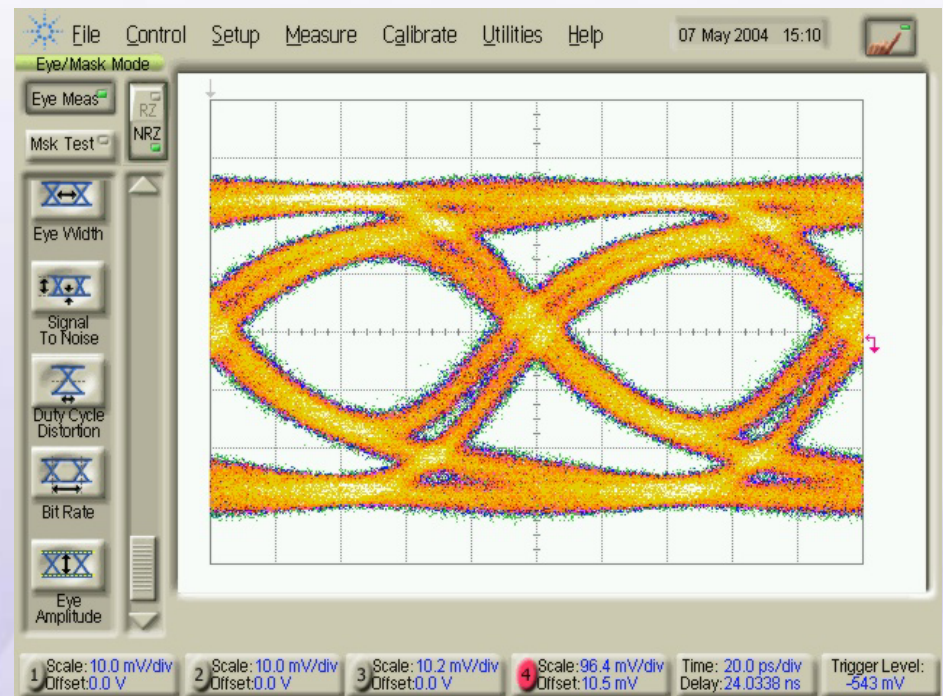
Waveform

Example of CML-based Comparator

- ◆ Aperture time compatible with 40Gb/s signal
- ◆ Operate with 10-GHz reduced-swing clock

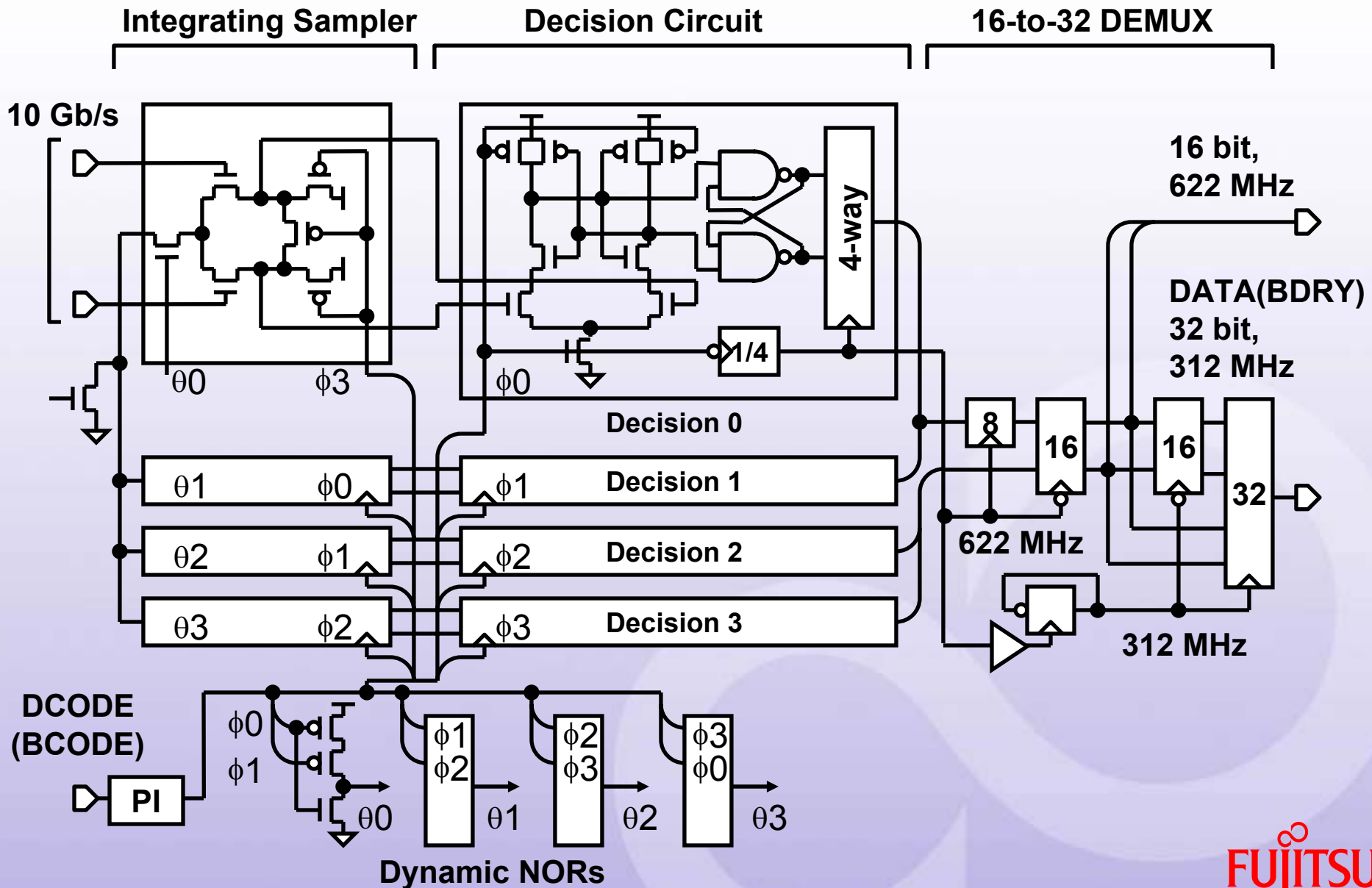


Output eye diagram



40Gb/s PRBS $2^{23}-1$ (BER < 10^{-12})

10Gb/s Rx Front end and DEMUX



10Gb/s MUX

32-to-4 MUX

4-to-1 MUX

Output stage

32 bit,
312 MHz

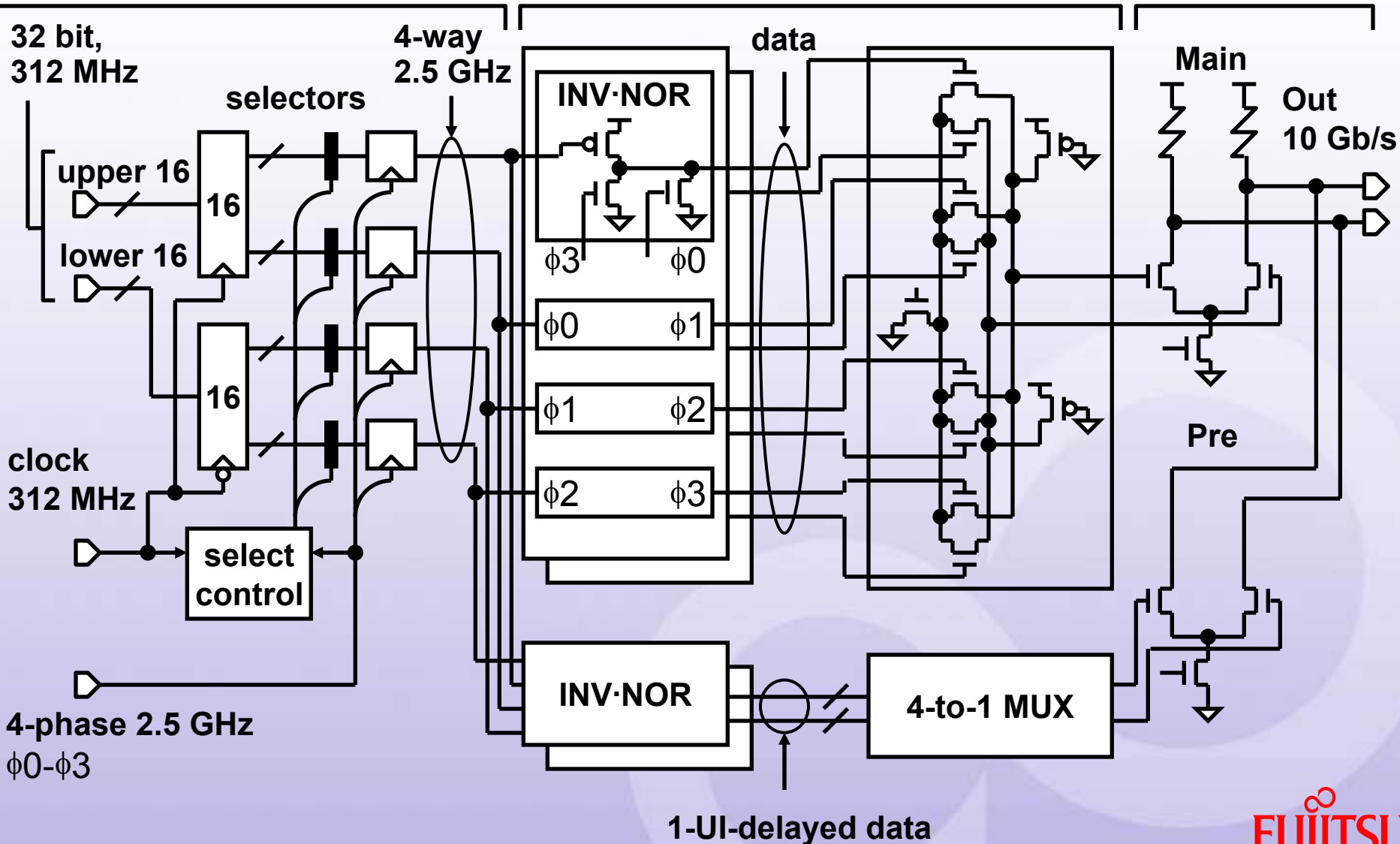
4-way
2.5 GHz

data

Main
Out
10 Gb/s

clock
312 MHz

4-phase 2.5 GHz
 $\phi 0-\phi 3$

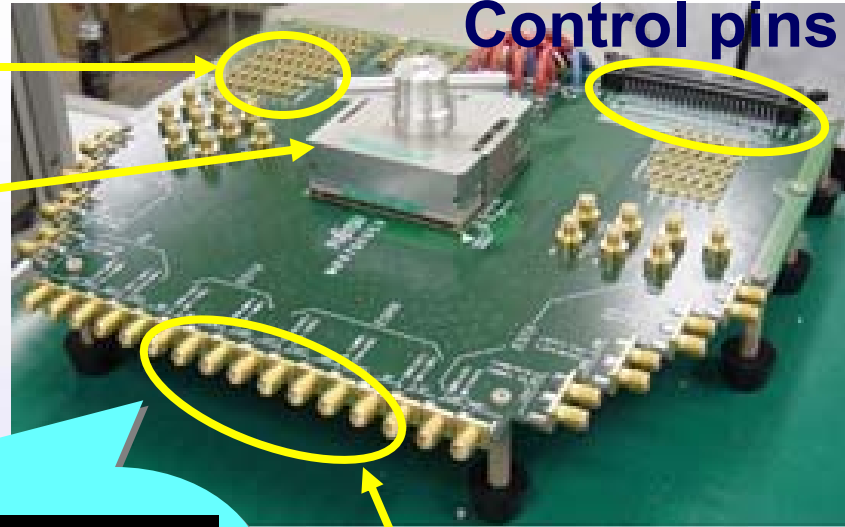


10Gb/s Transmitter Output Waveforms

High-speed monitor
signal pins

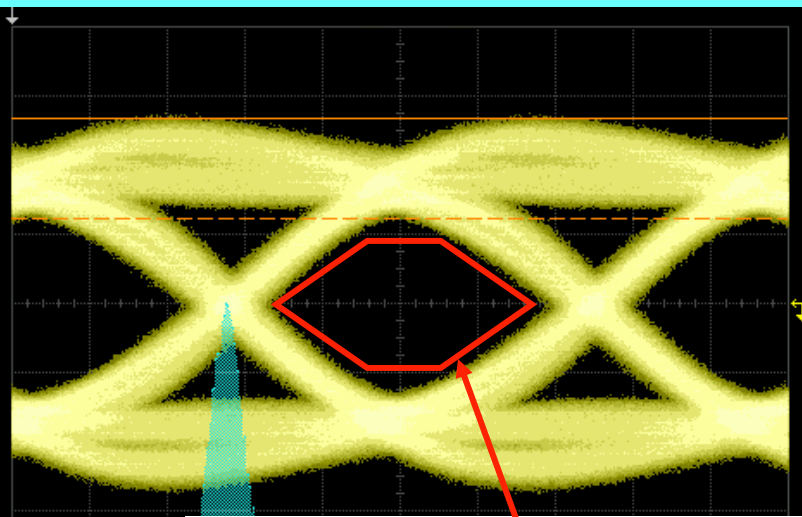
Socket

Control pins



Evaluation board

10Gb/s I/O pins



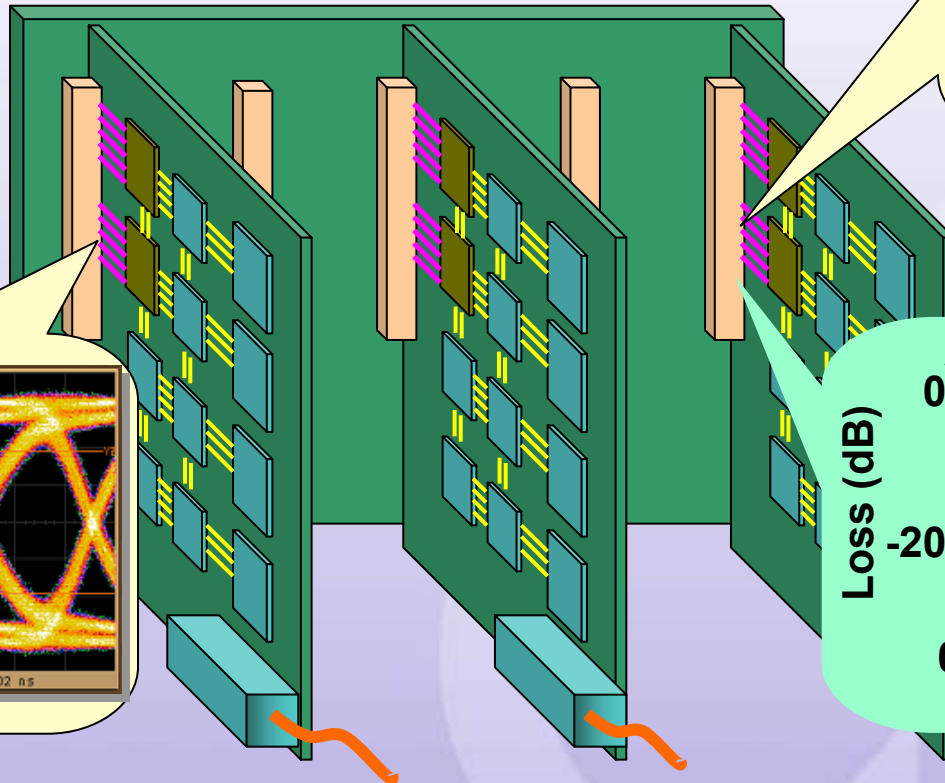
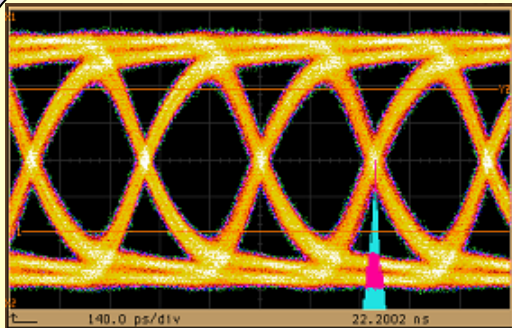
XFI(ASIC) eye template

Inter-symbol Interference (ISI) Compensation

Need to compensate for ISI due to signaling media

- Tx: Pre-emphasis
- Rx: Equalization

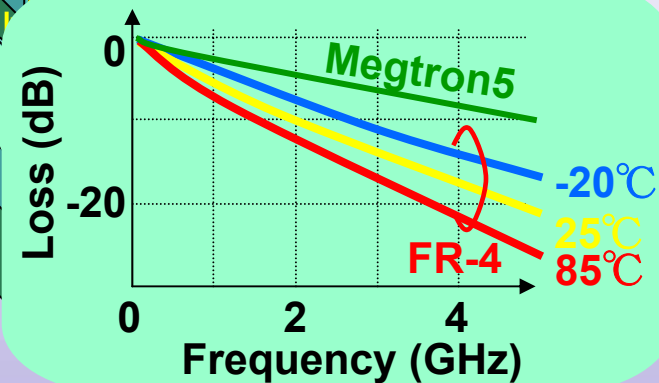
Tx



Rx

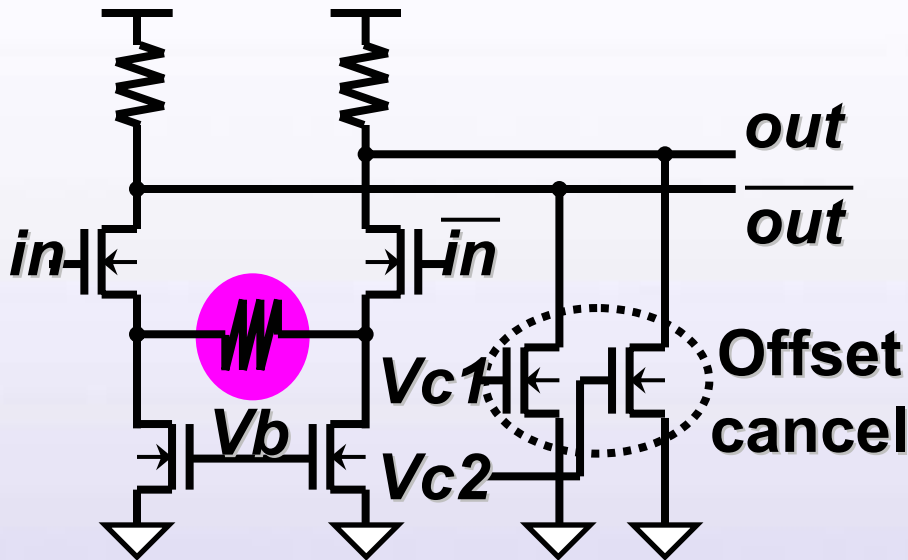


No opening in eye patterns

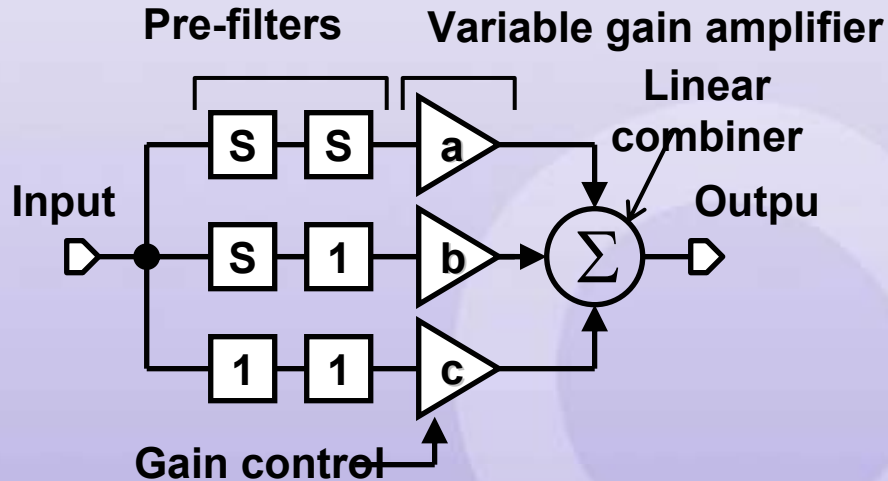
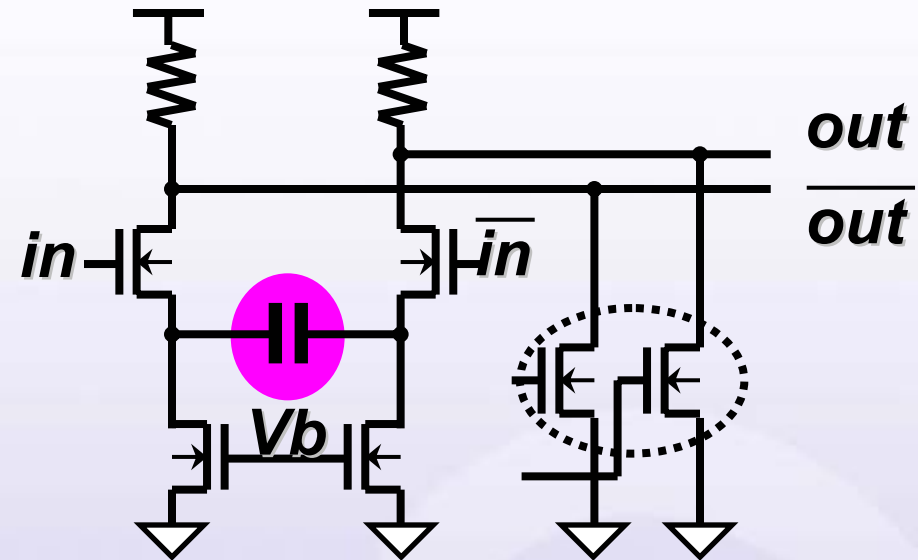


Second-order equalizer

“1” Flat gain over the signal BW

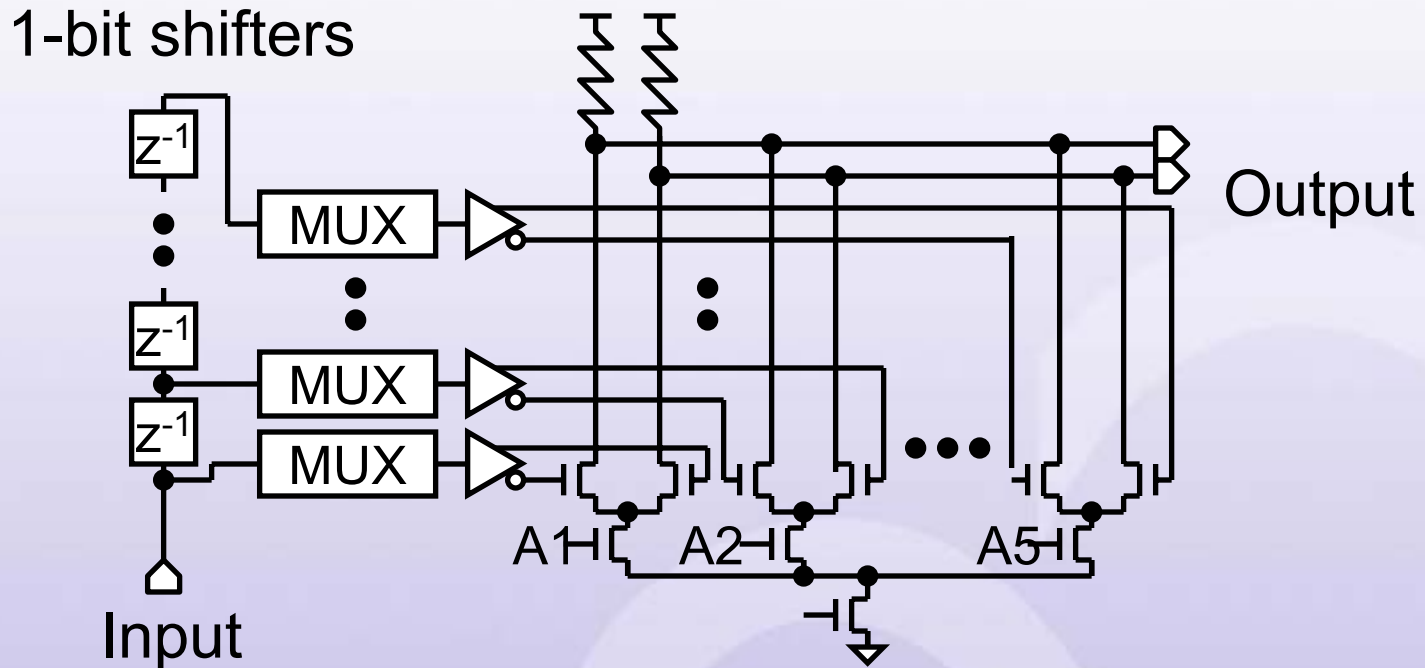


“S” Differentiator



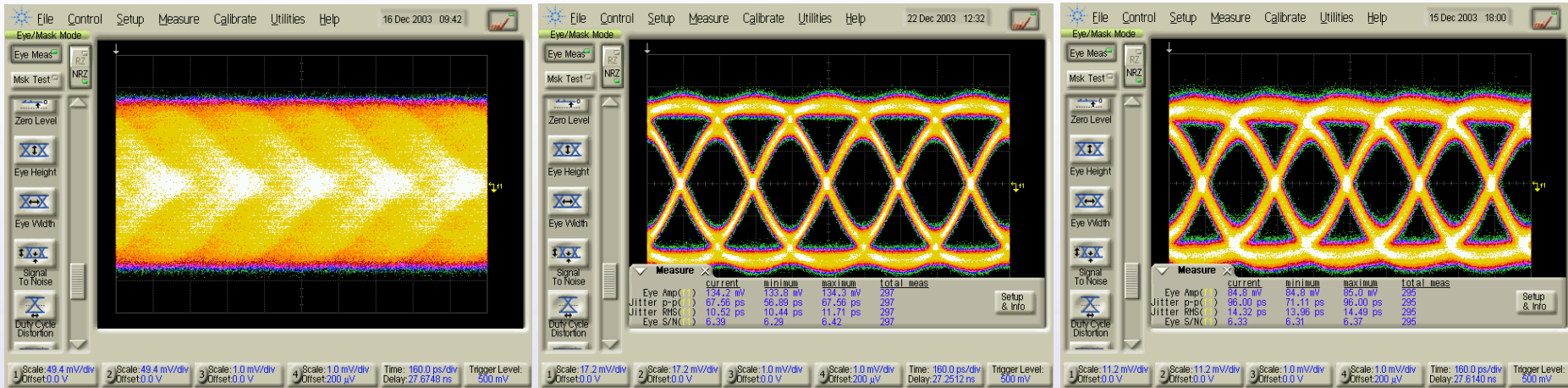
Transfer function :
 $H(s) = as^2 + bs + c$

Transmitter Equalizer (FIR filter)



Effects of Equalization

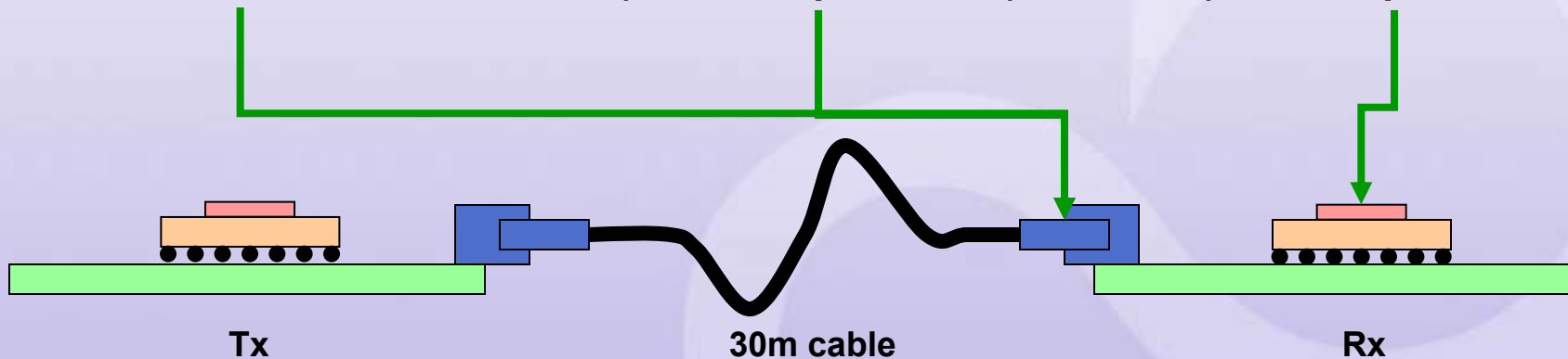
◆ 6.4Gb/s Transceiver with Tx FIR filter and Rx equalizer



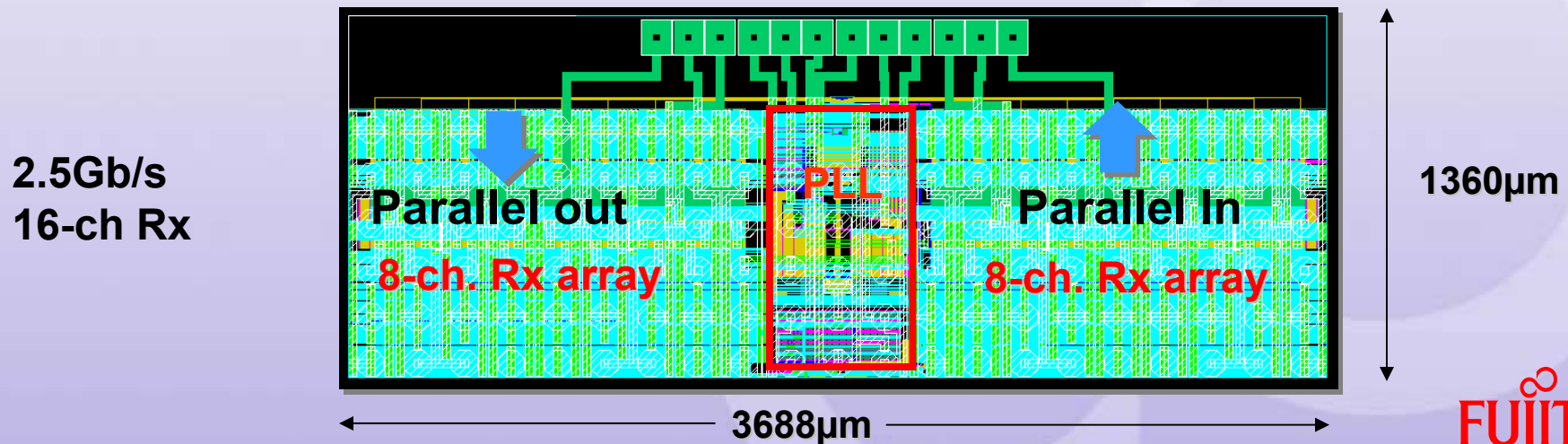
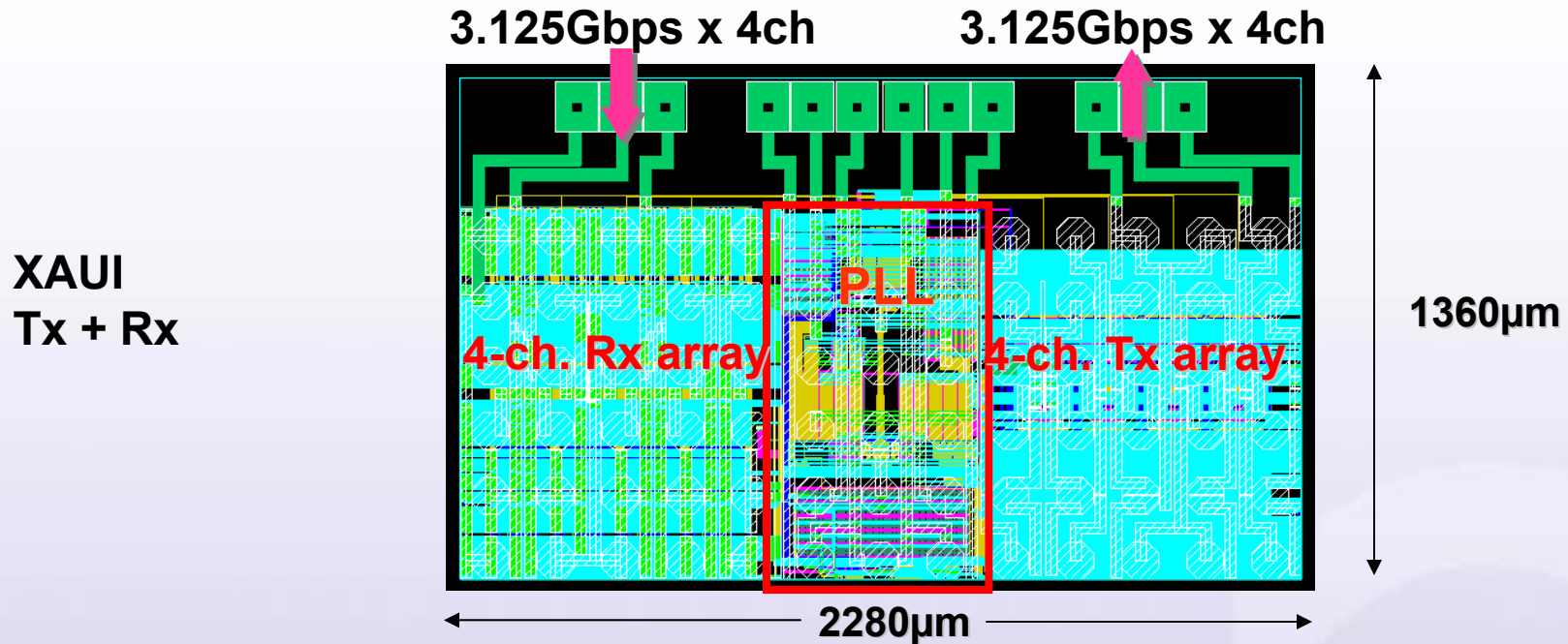
after 30m cable
(w/o Tx equalization)

after 30m cable
(with Tx equalization)

output of Rx equalizer
(w/o Tx equalization)



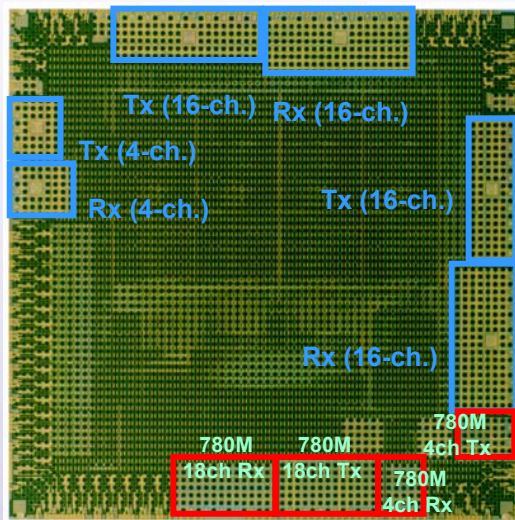
Example of Macro Layout



ASICs using High-Speed I/O Macros

0.18um

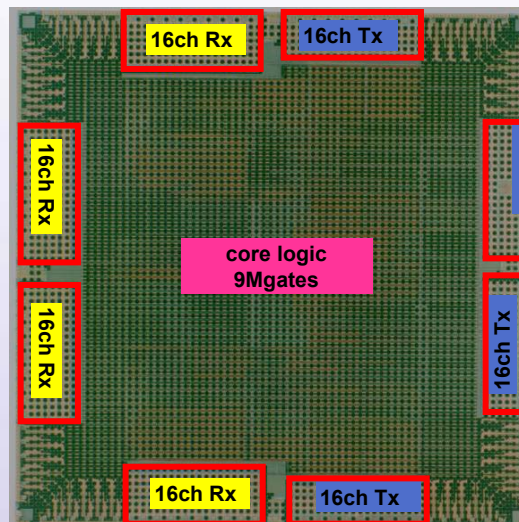
- 2.5Gbps x 72bit
- 780Mbps x 44bit



- Area: 14.962mm-sq
- Core logic: 7.5Mgates
- Package: FCBGA1225

0.18um

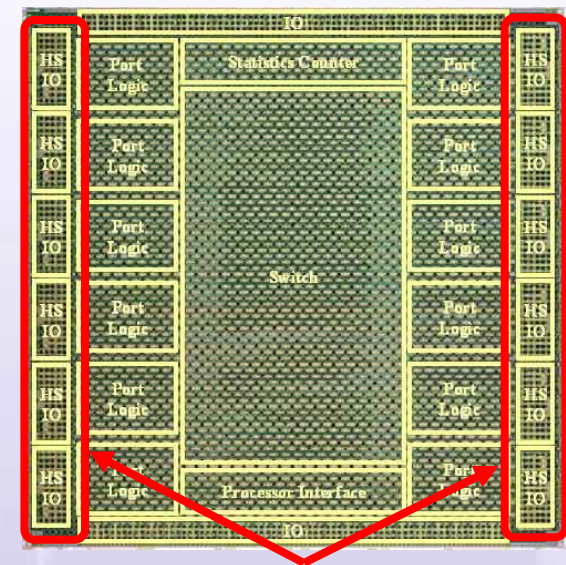
- 2.5Gbps x 128bit



- Area: 16.283mm-sq
- Core logic: 9Mgates
- Package: FCBGA1089

0.11um

- 3.125Gbps x 96bit



- Area: 16mm-sq
- XAUI(4x3.125Gbps) x12ports
- Package: FCBGA728

System-level evaluation done

Power Consumption (in 0.11 μ m CMOS)

**6.4 Gb/s transceiver (12-ch Tx, 12-ch Rx)
(with 5-tap Tx FIR filter + Rx equalizer)**

Tx channel	150 mW / channel
Rx channel	90 mW / channel
PLL	90 mW
Power per transceiver	255 mW/ch

10Gb/s transceiver (4-ch Tx, 4-ch Rx)

Tx channel	137 mW / channel
Rx channel	129 mW / channel
PLL	15 mW
5-GHz buffer / etc.	75 mW
Power per transceiver	311 mW/ch

Outline

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- ◆ Pin-bandwidth bottleneck

◆ Circuit solutions for bandwidth bottleneck

- ◆ Clock recovery scheme

- ◆ Receiver and transmitter front ends

◆ High-speed-I/O Future trends

CMOS High-speed I/O Speed Prediction

* IEEE Micro, January/February 1998,
pp12-pp24

1. Clock period

- Limited by clock tree bandwidth
- Minimum period T_{\min} : 8 x (FO-4 delay) for FO4 inverter chain

2. Transmitter unit interval

- Minimum unit Interval: 1x (FO-4 delay)

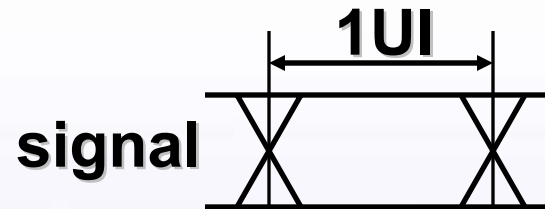
3. Receiver unit interval

- Minimum unit interleave: 1 x (FO-4 delay)

4. Overall performance

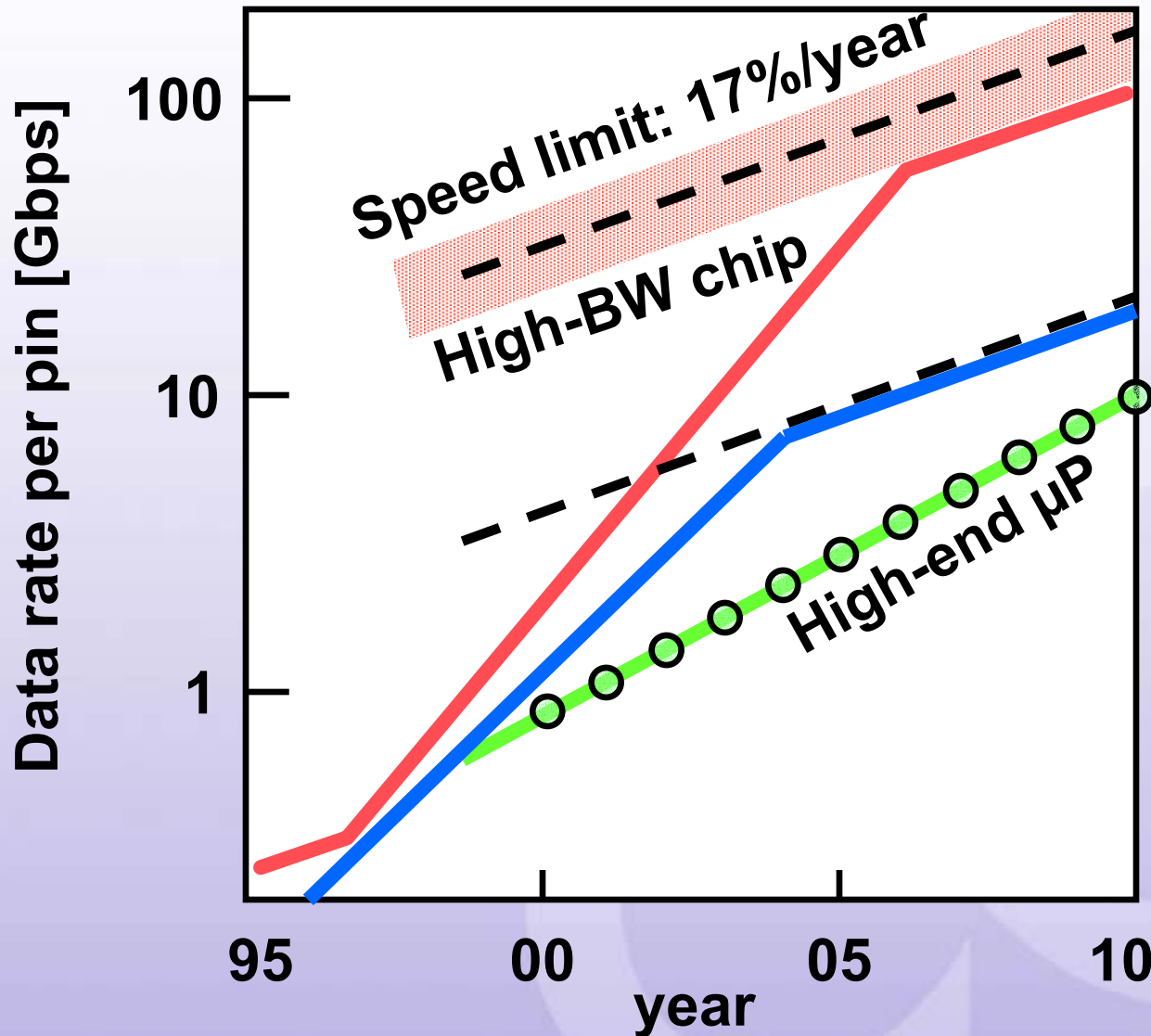
- Should use multi-phase clock
- Minimum unit time 1x (FO-4 delay) feasible

Speed Estimation for 0.11 μ m CMOS



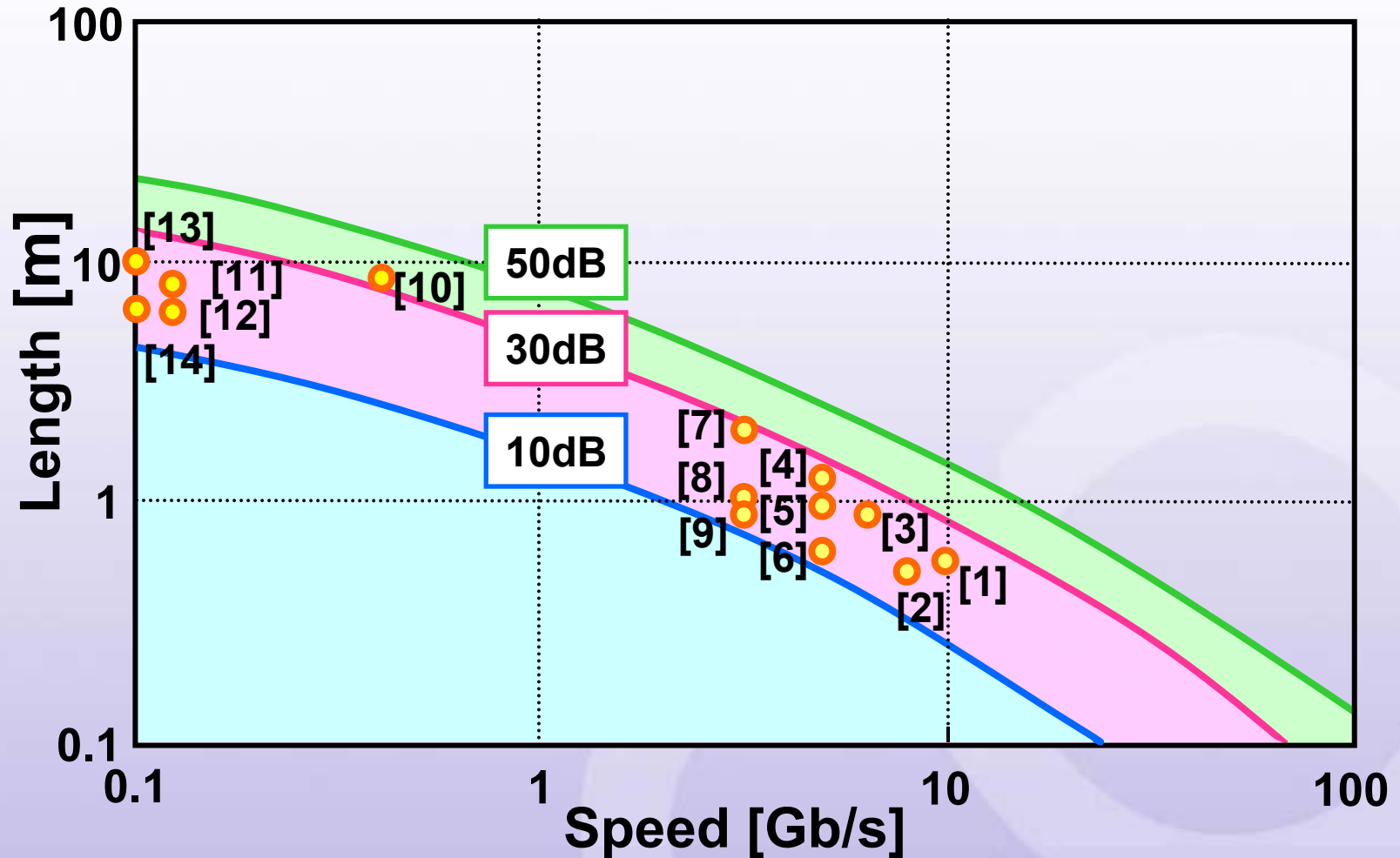
Item		Minimum 1UI value		@0.11 μ m
components	CMOS Logic Clock period	chip	16 x FO4 delay	610 ps
		local	8 x FO4 delay	300 ps
	Tx bit time (UI)	1 x FO4 delay		40 ps
	Rx bit time (UI)	latch	4 x FO4 delay	150 ps
		total	1 x FO4 delay@4-way	40 ps
Total	Bit time (UI)	1 x FO4 delay		40 ps

End of Moore's Law (for High BW CMOS)



Optical or Electric?

Back plane (FR4 model)



Conclusions

- ◆ **Exponential growth in CMOS IC performance**
 - ◆ High-speed I/O emergence was inevitable
- ◆ **Limitation in exponential trend**
 - ◆ Cannot sustain the exponential growth forever
 - ◆ Need new wiring topology for high-end extreme
 - ◆ Low power, ease of use, etc required for low end
- ◆ **A big picture needed to decide what to do now**

Backup Slides

Reference (Optical or Electric?)

CMOS, 2-PAM. Rx Equalizers

- [1] Y. Tomita et al., "A 10Gb/s Receiver with Equalizer and On-chip ISI Monitor in 0.11 μ m CMOS," in IEEE Symp. VLSI Circuits Dig. Tech. Papers, Feb. 2004, pp. 202-205.
- [2] R. Farjad-Rad et al., "0.622-8.0Gbps 150mW Serial IO Macrocell with Fully Flexible Preemphasis and Equalization," in IEEE Symp. VLSI Circuits Dig. Tech. Papers, Feb. 2003, pp. 63-66.
- [3] H. Higashi et al., "5-6.4 Gbps 12 channel Transceiver with Pre-emphasis and Equalizer," in IEEE Symp. VLSI Circuits Dig. Tech. Papers, Feb. 2004, pp. 130-133.
- [4] J. S. Choi et al., "A 0.18- μ m CMOS 3.5-Gbps Continuous-Time Adaptive Cable Equalizer Using Enhanced Low-Frequency Gain Control Method," IEEE J. Solid-State Circuits, vol. 39, pp. 419-425, Mar. 2004.
- [5] Y. Kudoh et al., "A 0.13- μ m CMOS 5-Gb/s 10-meter 28AWG cable transceiver with no-feedback-loop continuous-time post-equalizer," in IEEE Symp. VLSI Circuits Dig. Tech. Papers, Feb. 2002, pp. 64-67.
- [6] V. Stojanovic et al., "Adaptive Equalization and Data Recovery in a Dual-Mode (PAM2/4) Serial Link Transceiver," in IEEE Symp. VLSI Circuits Dig. Tech. Papers, Feb. 2004, pp. 348-351.
- [7] W. Gai et al., "A 4-Channel 3.125Gb/s/ch CMOS Transceiver with 30dB Equalization," in IEEE Symp. VLSI Circuits Dig. Tech. Papers, Feb. 2004, pp. 138-141.
- [8] H. Wang et al., "A Quad Multi-speed Serializer/Deserializer with Analog Adaptive Equalization," in IEEE Symp. VLSI Circuits Dig. Tech. Papers, Feb. 2004, pp. 340-343.
- [9] M. Q. Le et al., "A 3.125Gbps Timing and Data Recovery Front-end with Adaptive Equalization," in IEEE Symp. VLSI Circuits Dig. Tech. Papers, Feb. 2004, pp. 344-347.
- [10] A. J. Baker, "An Adaptive Cable Equalizer for Serial Digital Video Rates to 400Mb/s," in IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers, Feb 1996, pp. 174-175.
- [11] J. N. Babanezhad, "A 3.3V Analog Adaptive Line-Equalizer For Fast Ethernet Data Communication," in Proc. IEEE Custom Integrated Circuit Conf., May 1998, pp. 343-346.
- [12] T-C. Lee et al., "A 125-MHz CMOS Mixed-Signal Equalizer for Gigabit Ethernet on Copper Wire," in Proc. IEEE Custom Integrated Circuit Conf., May 2001, pp. 131-134.
- [13] A. Shoal et al., "A CMOS Mixed-Signal 100Mb/s Receive Architecture for Fast Ethernet," in Proc. IEEE Custom Integrated Circuit Conf., May 1998, pp. 253-256.
- [14] O. Shoaie et al., "A 3V Low-Power 0.25 μ m CMOS 100Mb/s Receiver for Fast Ethernet," in IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers, Feb 2000, pp. 308-309.

Injection locking

◆ Well-known phenomena in oscillators

- ◆ Oscillator is synchronized with an injected clock signal if the injection frequency is close to the free running frequency of the oscillator

◆ Analysis methods

- ◆ Adler equation (R. Adler, Proc IRE, vol34, p.351, 1946)

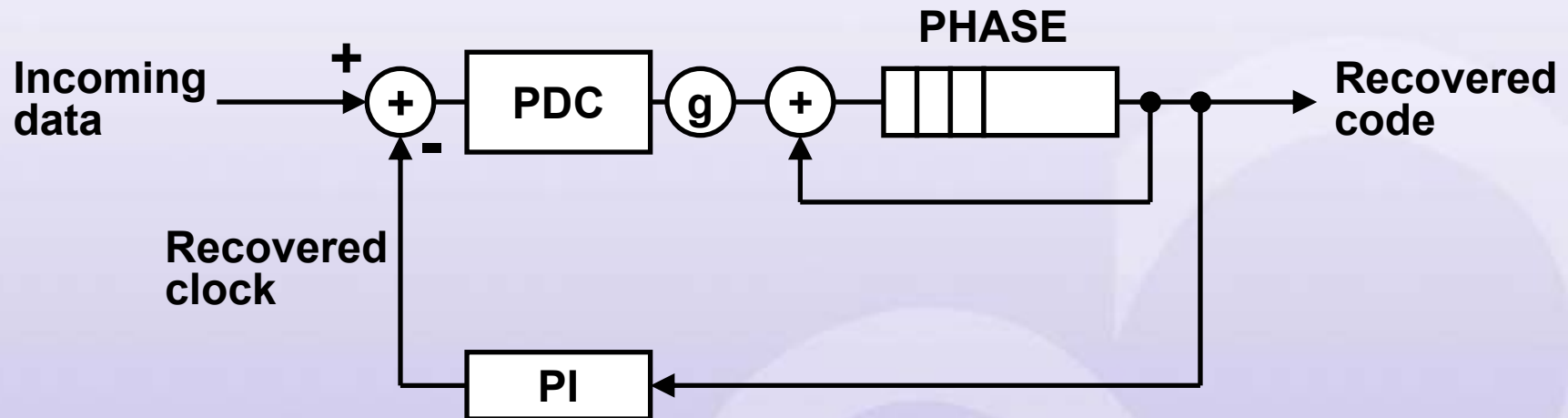
$$\frac{d\theta}{dt} = \omega_0 + \frac{\omega_0}{2Q} \frac{A_{inj}}{A} \sin(\theta_{inj} - \theta)$$

- ◆ non-linear perturbation analysis (A. Demir et al, IEEE Tans. Circ. And Syst. -I, vol.47, p655, 2000)

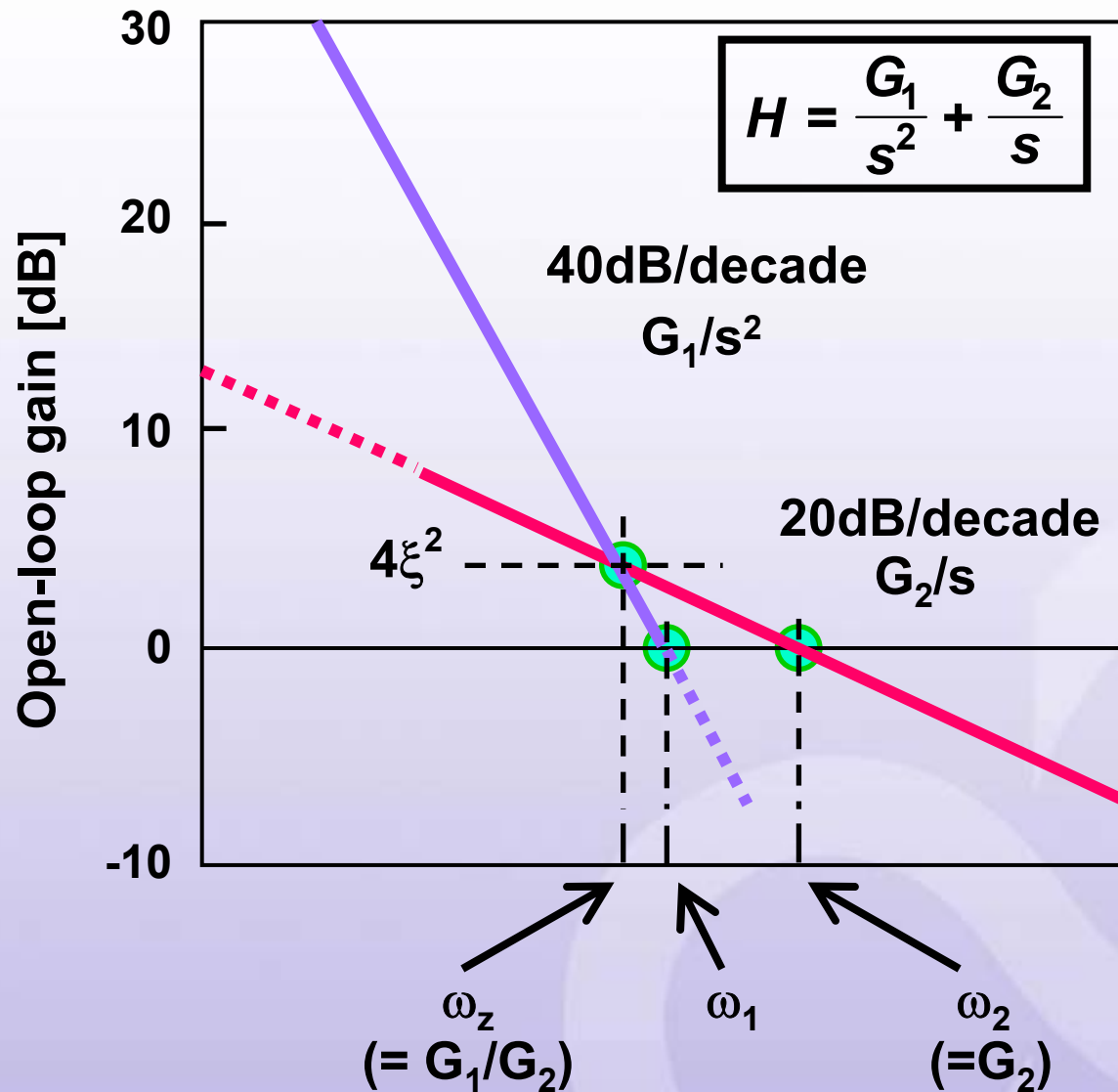
$$\frac{d\theta}{dt} = \varepsilon \gamma(t + \theta(t)) n(t)$$

First-order feedback loop

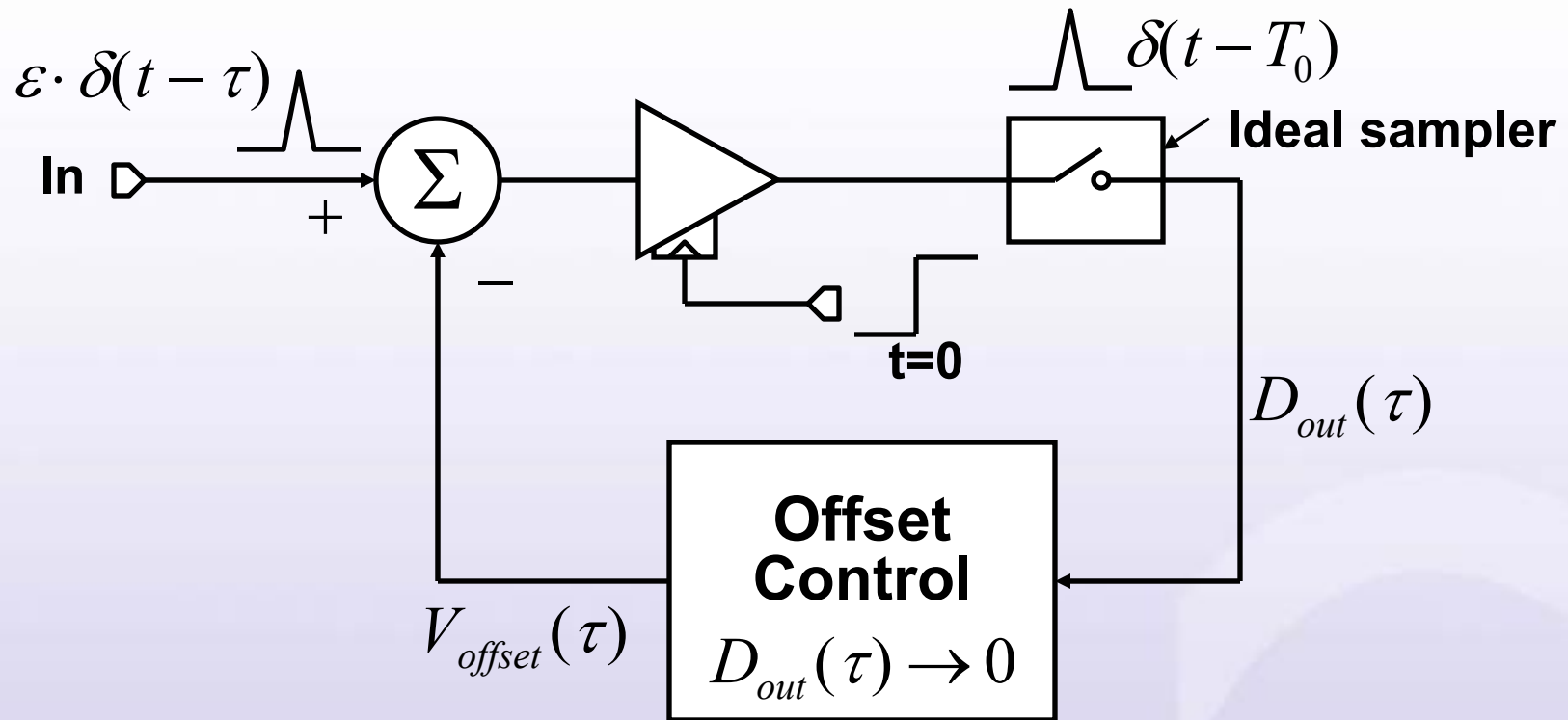
- ◆ Phase error is integrated into the phase register
 - ◆ No phase error for static phase error (skew)
 - ◆ Tracking error for dynamic phase error (i.e., frequency difference)



Open-loop Gain of Second-Order Loop



Sampling Function Calculation

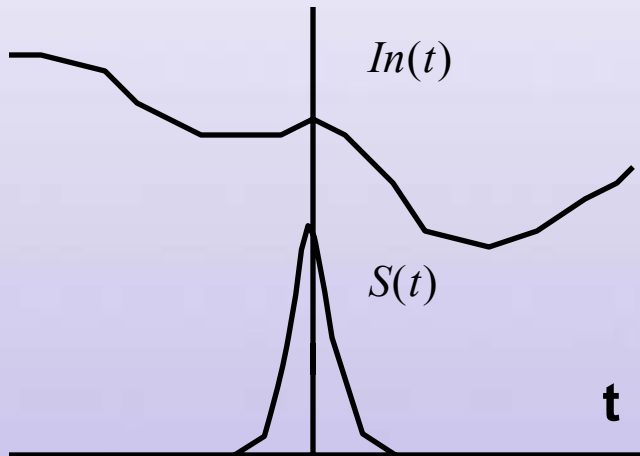
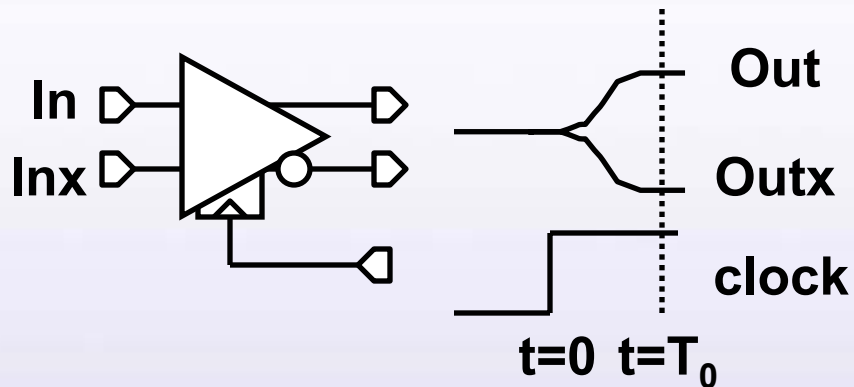


Input referenced
sampling function

$$S(\tau) = \frac{V_{offset}(\tau)}{\varepsilon}$$

Sampling Function

- ◆ Clock signal rises at $t=0$ and output observed at $t=T_0$



$$Out(t) = \int_{-\infty}^t h(t, \tau) In(\tau) d\tau$$

$$Out(T_0) = \int_{-\infty}^{T_0} h(T_0, \tau) In(\tau) d\tau$$

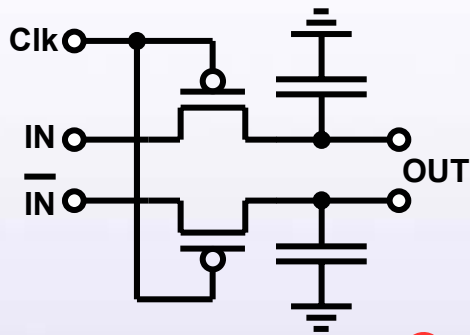
$$= \int_{-\infty}^{T_0} S(\tau) In(\tau) d\tau$$

$$\underline{S(\tau) \equiv h(T_0, \tau)}$$

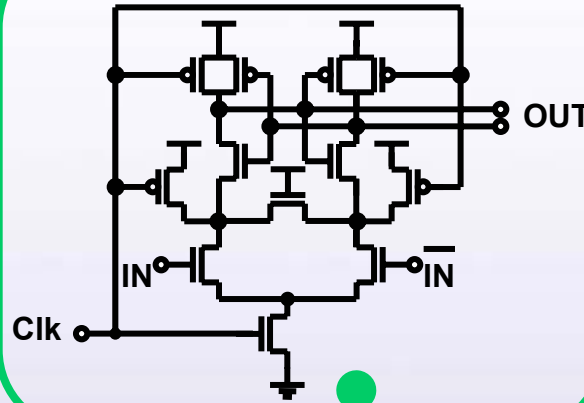
Sampling function

Sampling Function Example

PMOS switch



Strong-ARM latch



CML latch

