

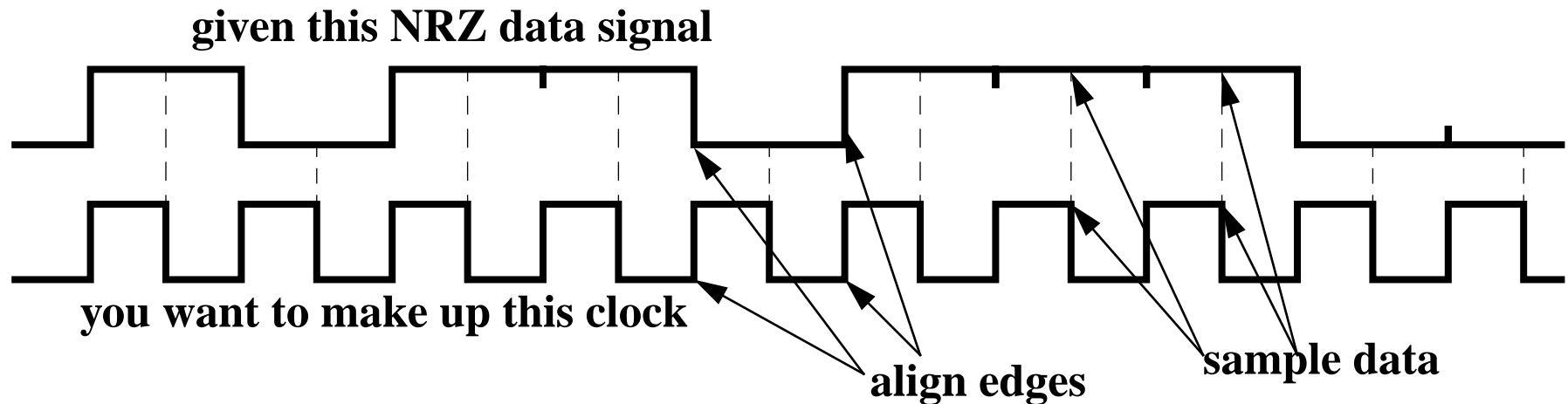
Clock Recovery Architecture for SONET Compliant WDM Transponder

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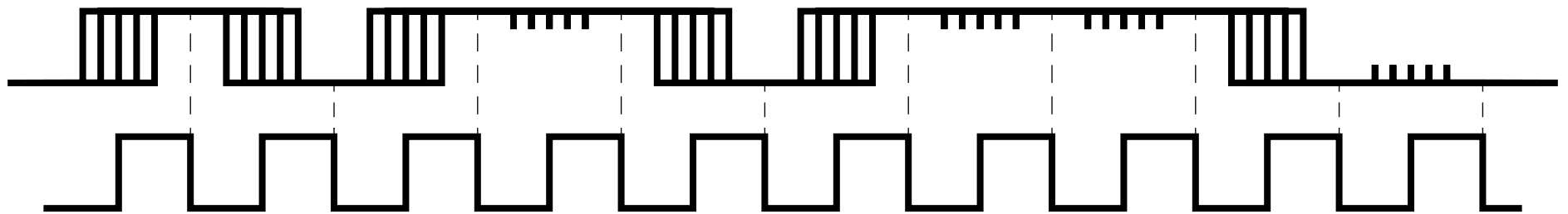
presented at
University of Toronto
4 October 2002
Toronto Ontario Canada

What is Clock Recovery ?



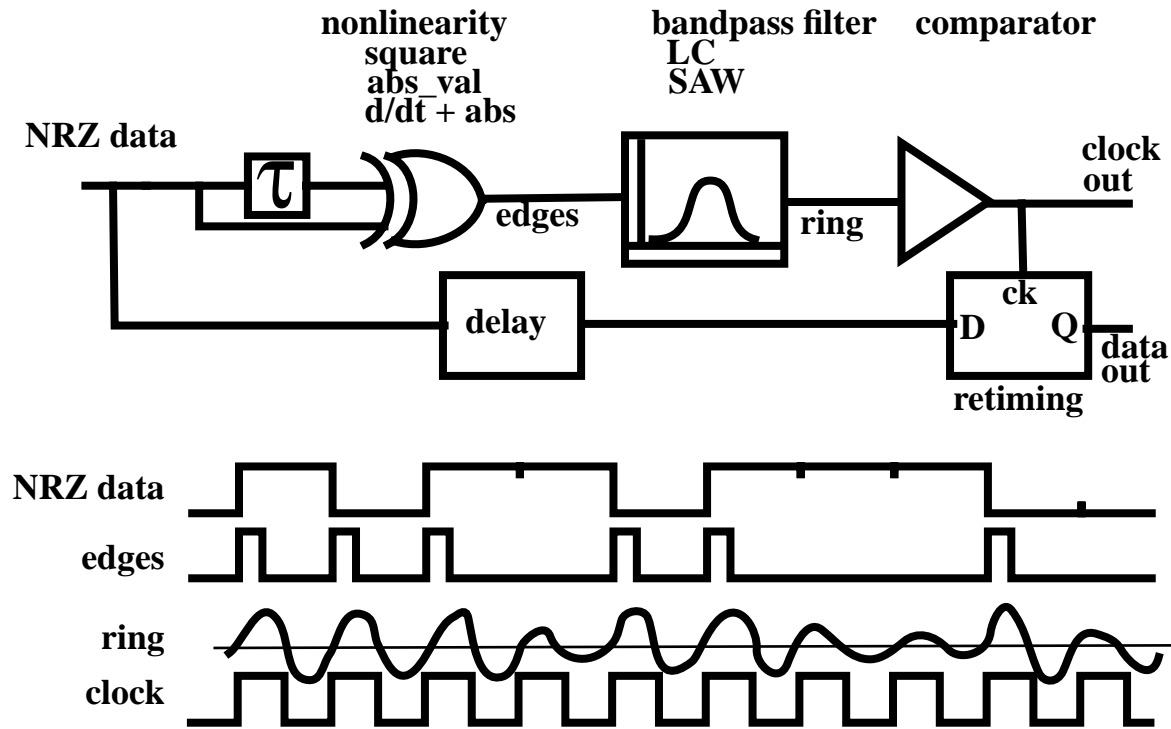
So, what is the problem ?

you usually don't get a nice, clean data signal
it is most likely corrupted with jitter and other impairments



but you still want to make up the same nice, clean clock !!

Ring Tank type of Clock Recovery



FATAL FLAW

A requirement of clock recovery is to produce a valid clock output signal even if there is a long string of transitionless data or Consecutive Identical Digits, CID. This is described in Appendix I to CCITT G.958. This is the **fatal** performance **flaw** of SAW based clock recovery techniques. Since a SAW is a narrow-bandpass filter, it cannot produce an output with no input. When input transitions cease, the filter will continue to produce a clock signal as it rings down; but eventually the clock signal will cease. A high Q for the bandpass will allow the clock to not fade away, but such a high Q places unreasonable demands on center frequency accuracy. In a SAW filter, if the center frequency is not correct, then static phase error results. While static phase must always be compensated in the retiming path of the SAW, the temperature stability of static phase due to center frequency drift of the bandpass is more difficult to accommodate. So the SAW bandpass Q must be limited to a value which allows premature fading of the clock with a long string of transitionless data.

advantages

- guaranteed frequency acquisition
- fast acquisition

problems

- expensive: need accurate center frequency
- ringdown phase drift during CID
- clock loss on long CID
- phase matching delay over temperature

Ringing Tank type of Clock Recovery

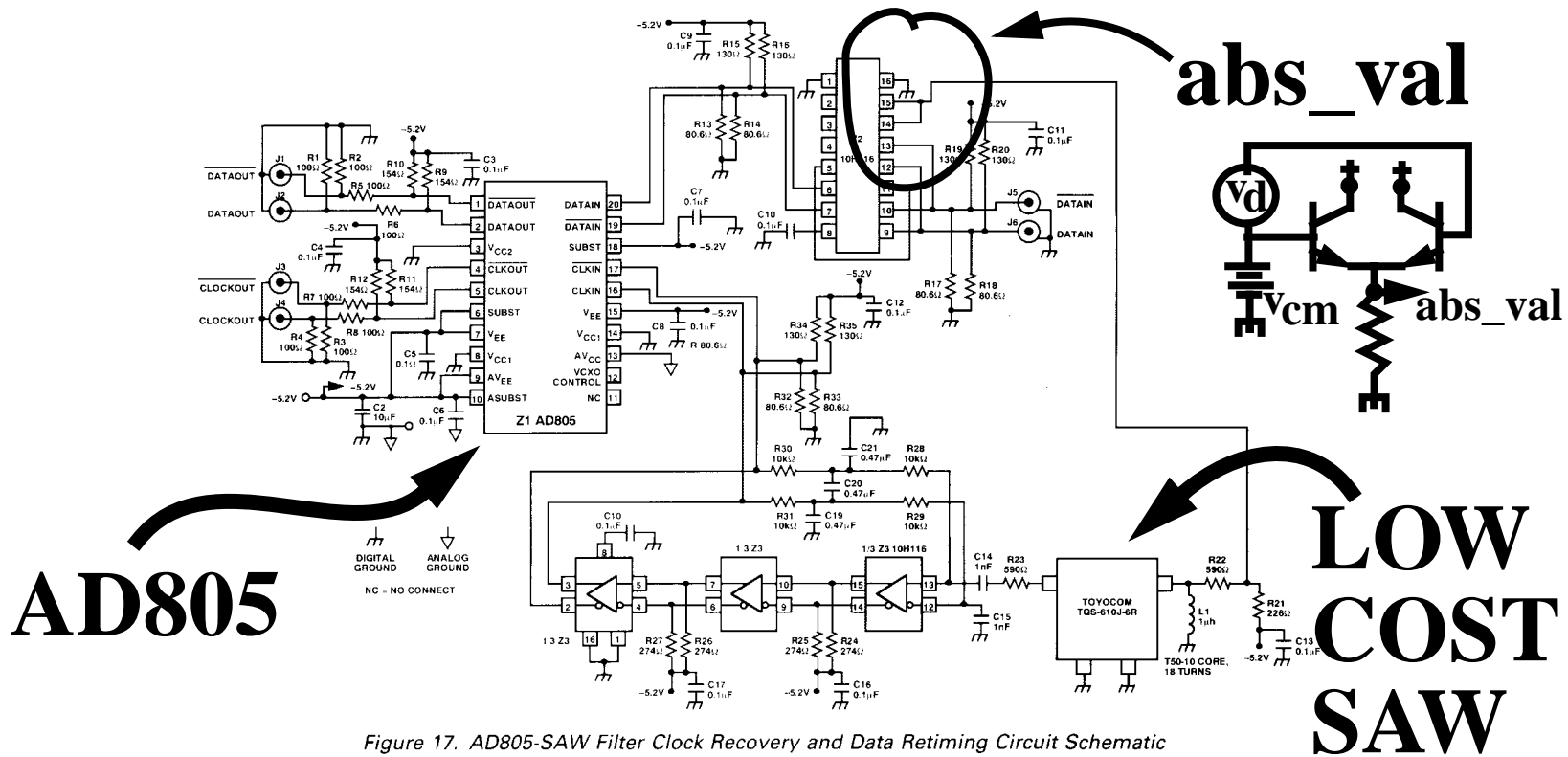
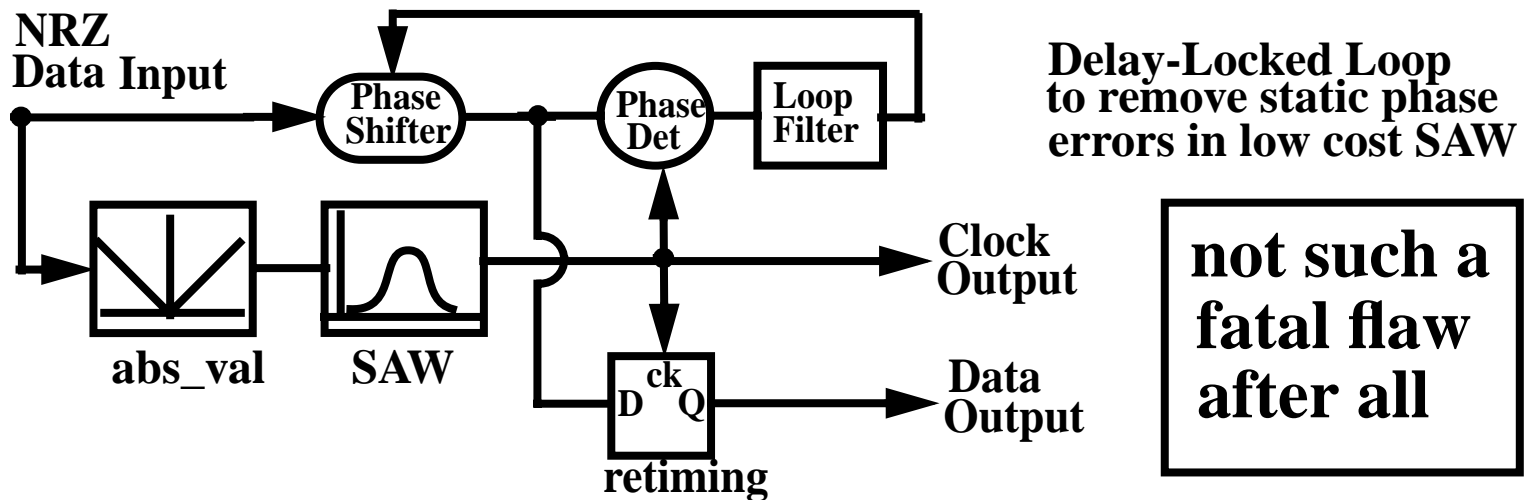
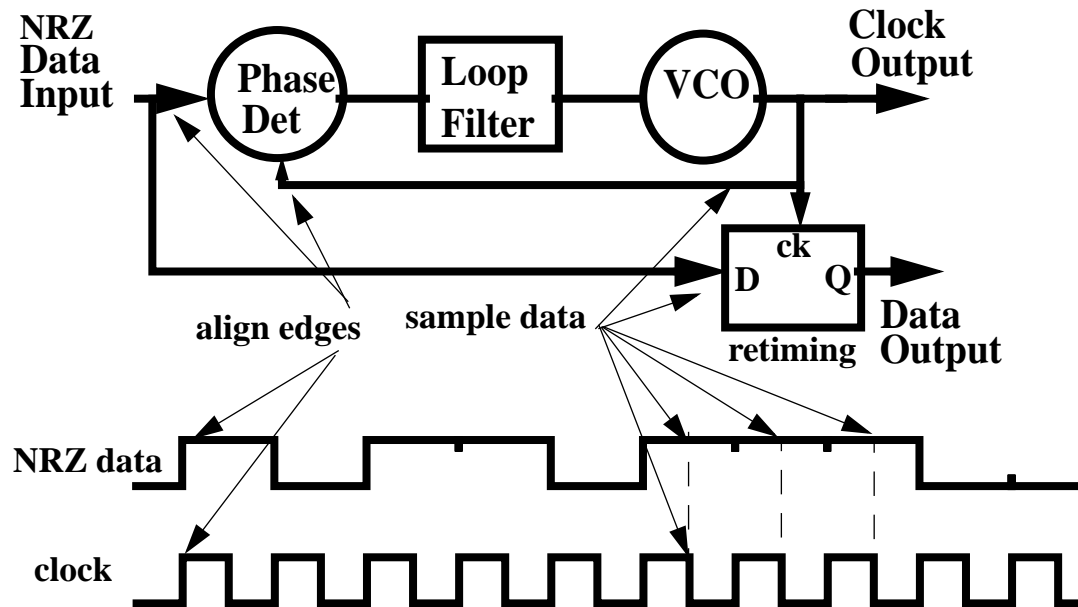


Figure 17. AD805-SAW Filter Clock Recovery and Data Retiming Circuit Schematic



Phase-Locked Loop type of Clock Recovery



advantages

free running clock on long CID

low cost

problems

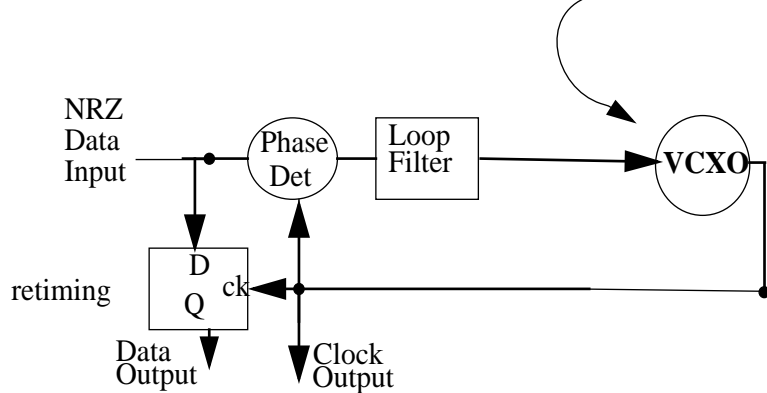
frequency acquisition not guaranteed: need acquisition aid

false lock to data sidebands possible

possible injection lock to power supply noise

Frequency Acquisition Aid

Voltage Controlled Crystal Oscillator



CRYSTAL OSCILLATOR

advantages

simple

very low jitter generation

problems

expensive

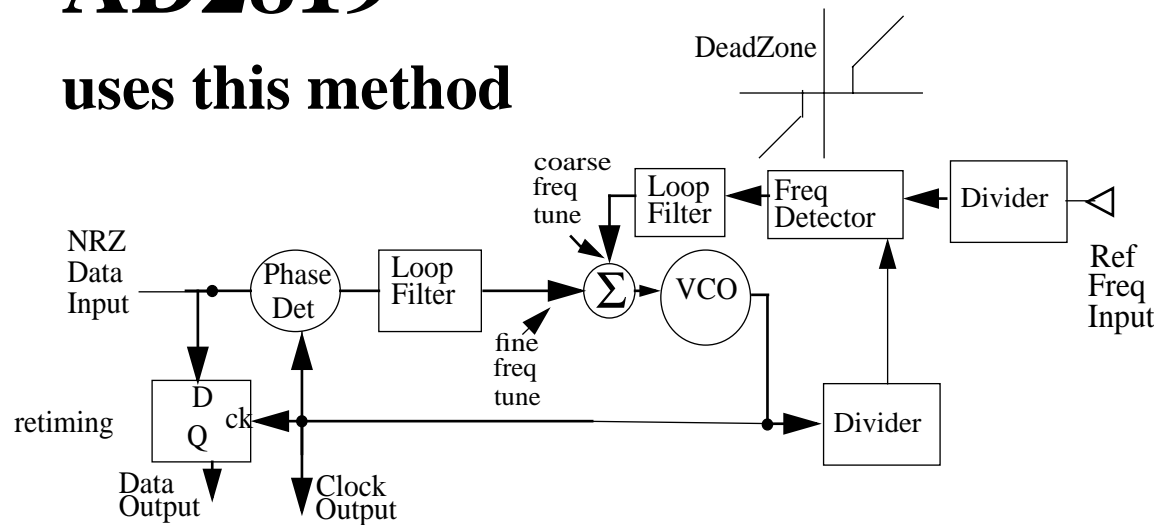
large size

jitter tolerance not good

limited frequency range

AD2819

uses this method



SYNTHESIZER

with

DEADZONE

advantages

simple

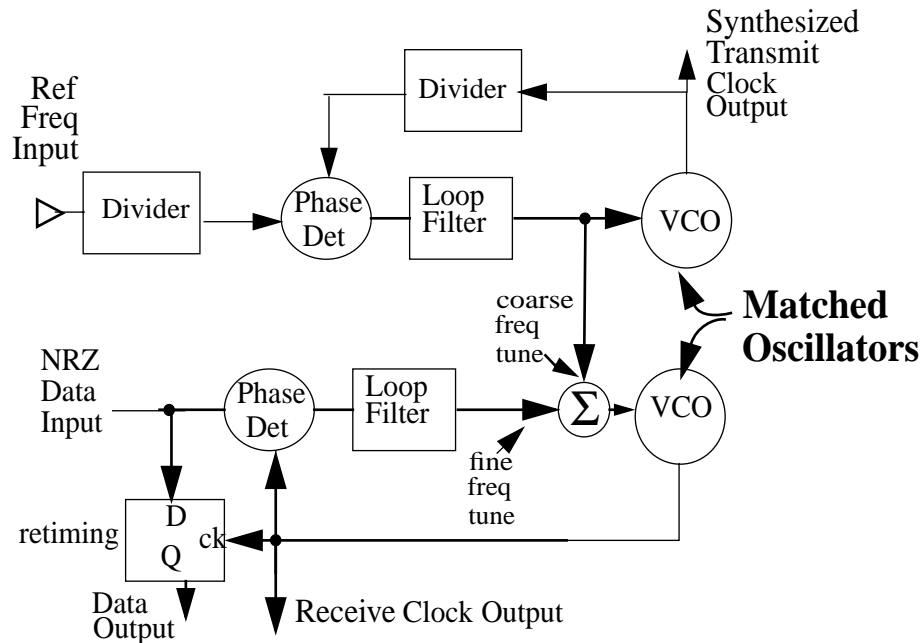
problems

need reference frequency

need extra loop filter

need deadzone in freq det

Frequency Acquisition Aid



SYNTHESIZER with MATCHED OSCILLATORS

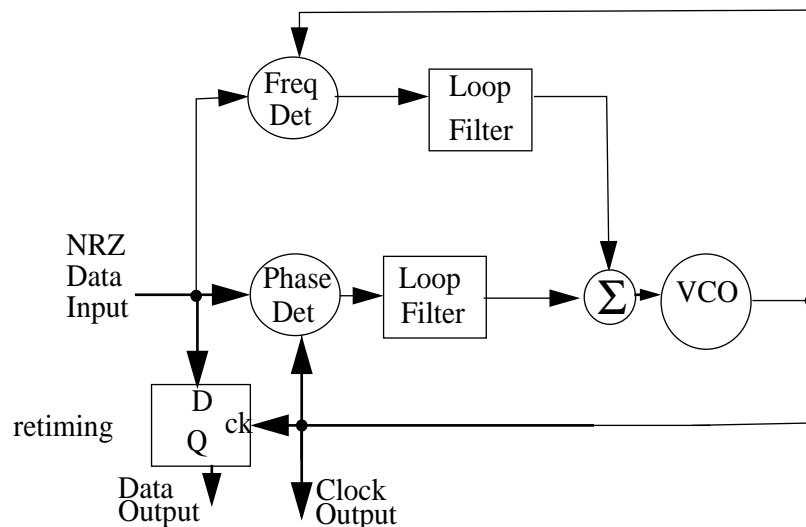
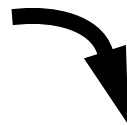
advantages

provides synthesized transmit clock

problems

need reference frequency
need extra loop filter
two VCO may entrain
too many moving parts

AD807, AD808 use this method



FREQUENCY DETECTOR

advantages

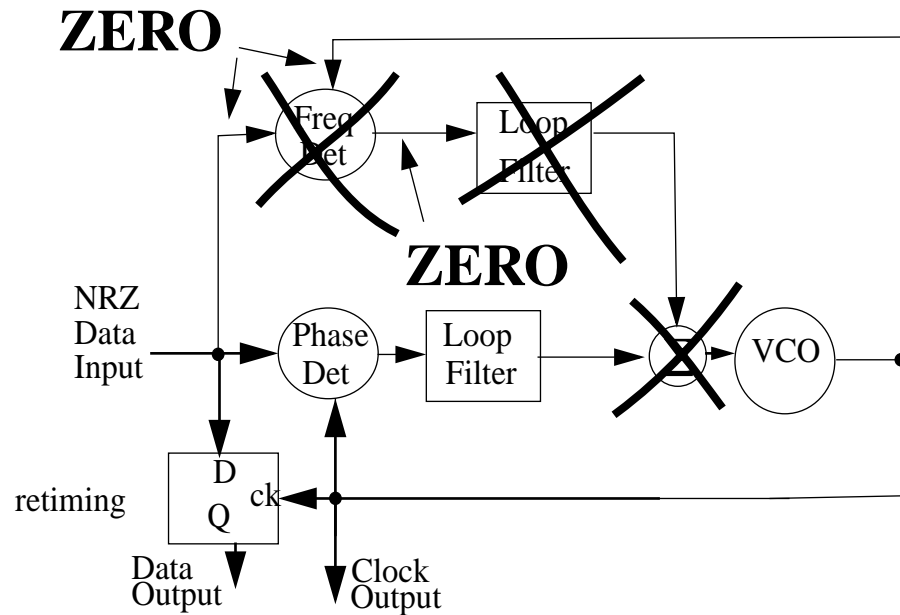
simple

no external reference clock
two loop filters can merge

problems

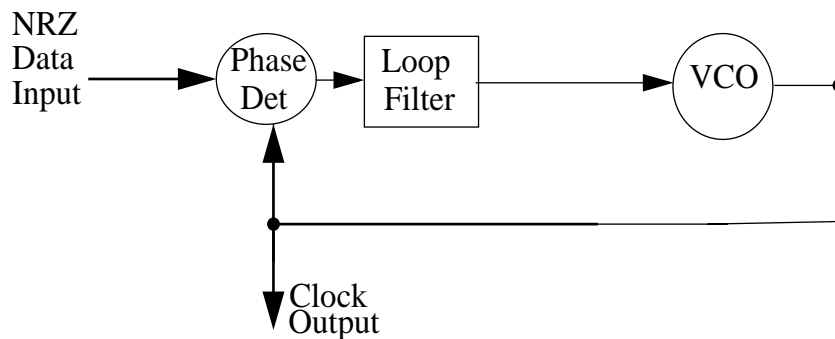
need frequency detector which tolerates data
need frequency detector which tolerates jitter

Simplified Model while in Phase-Lock



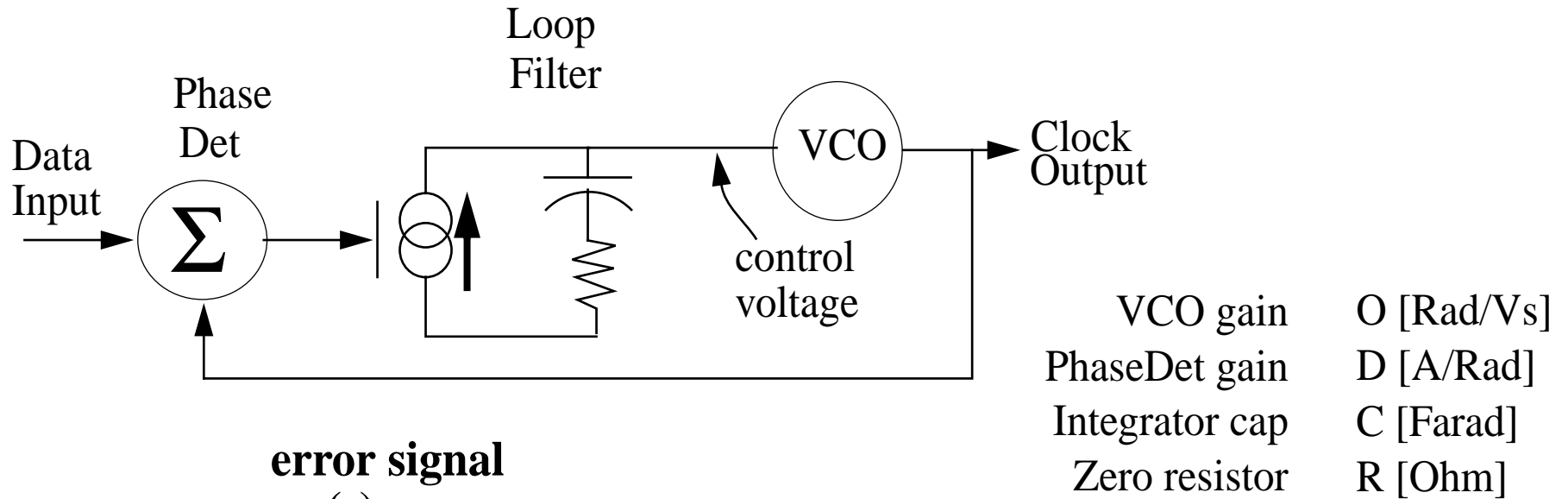
In lock the frequency difference is ZERO!

So the frequency detector can be neglected



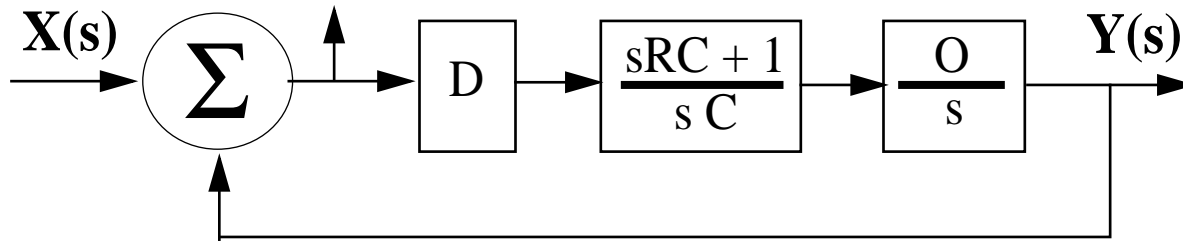
This leaves just a very simple model of the phase-locked loop.

Simplified Model while in Phase-Lock



error signal

$e(s)$



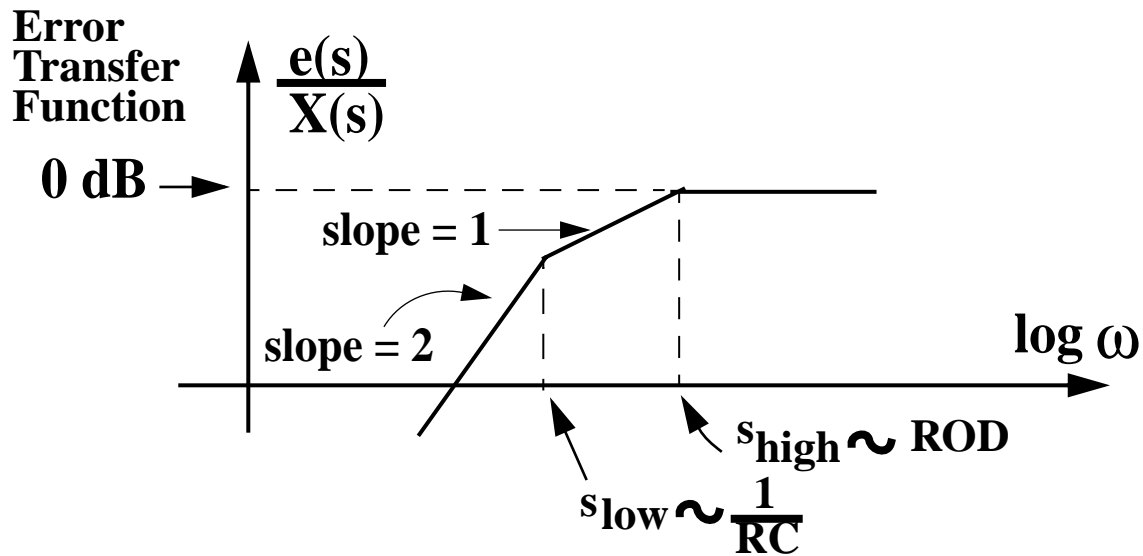
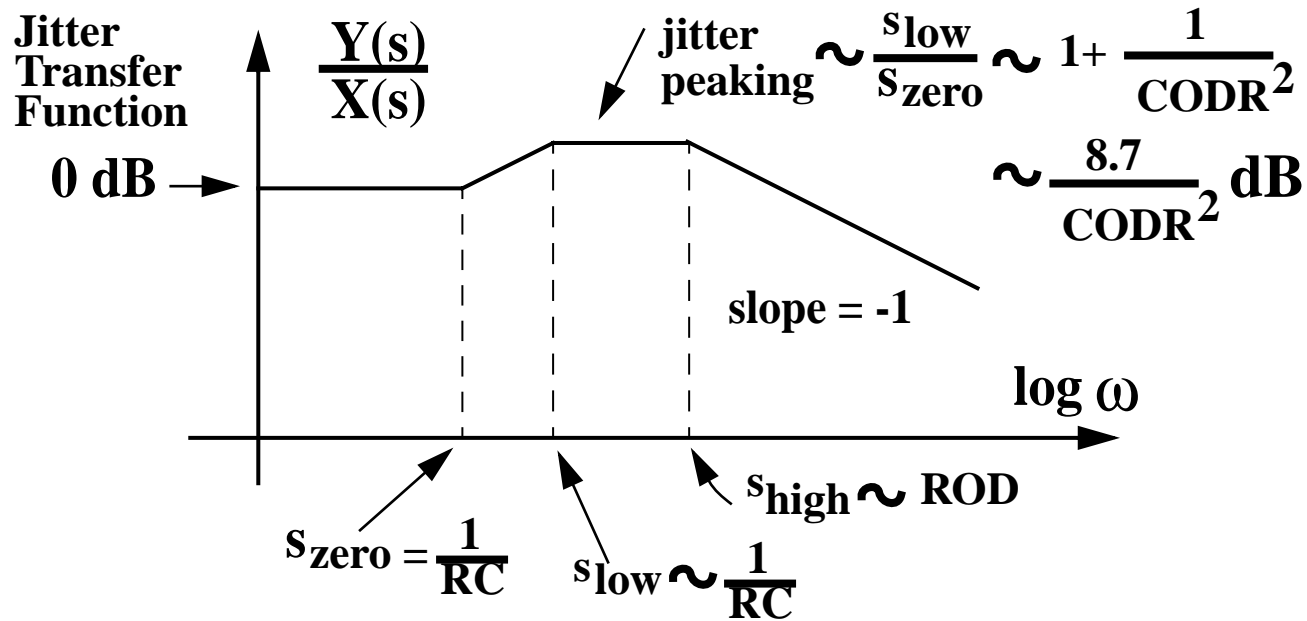
$$\frac{Y(s)}{X(s)} = \frac{sRC + 1}{s^2 \frac{C}{OD} + sRC + 1}$$

Jitter Transfer

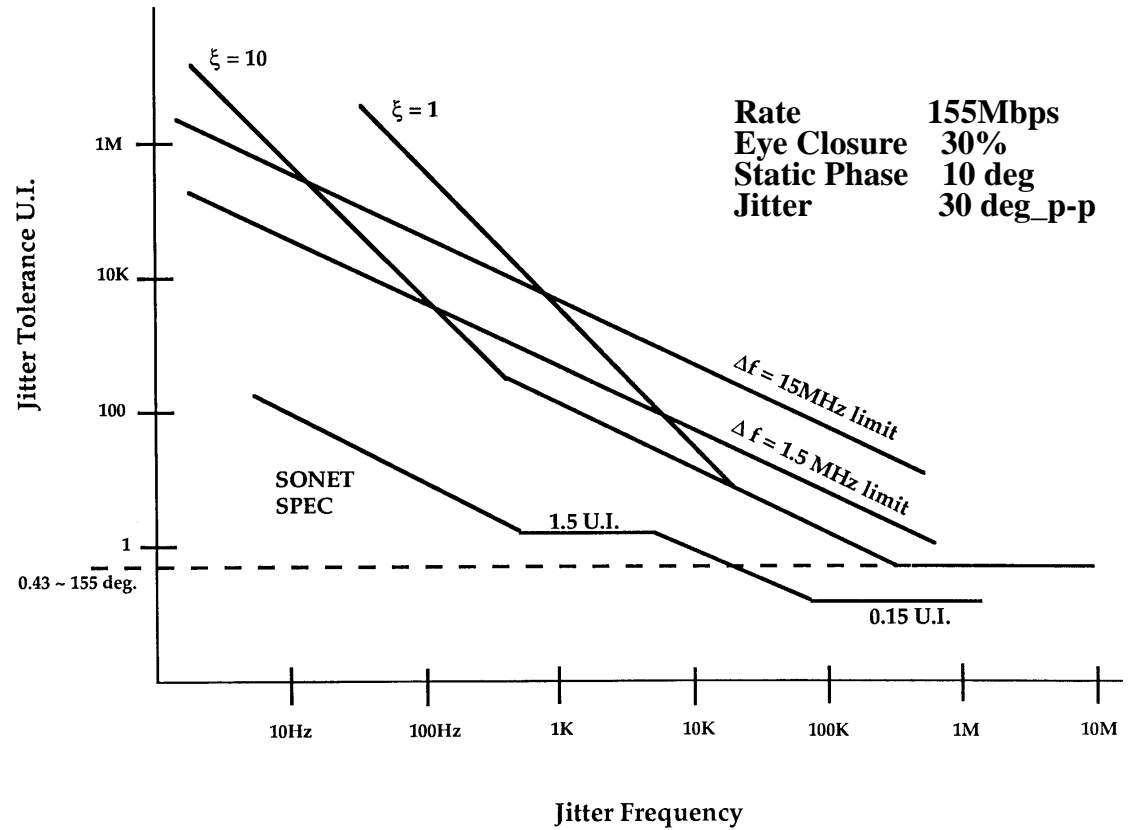
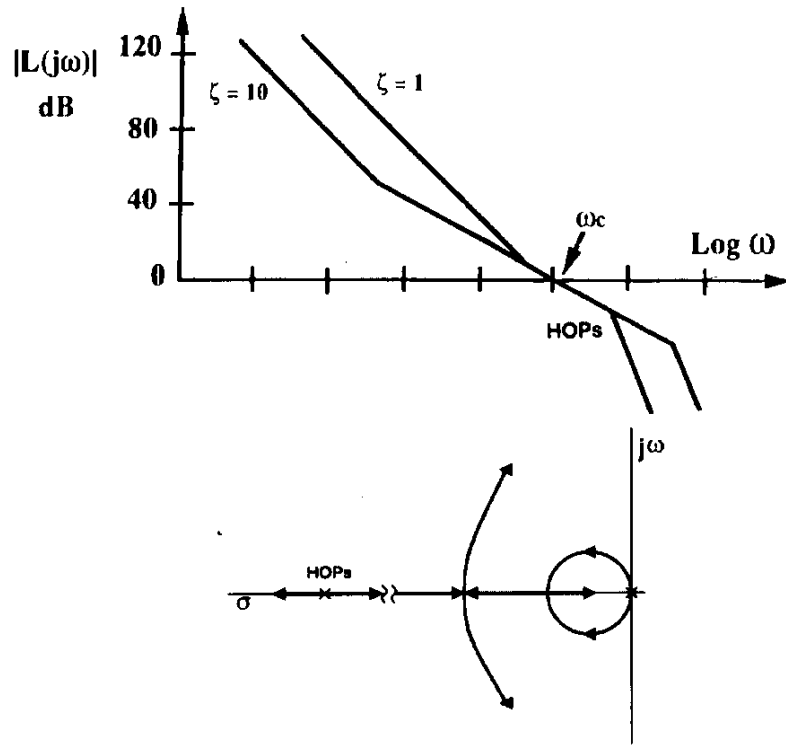
$$\frac{e(s)}{X(s)} = \frac{s^2}{s^2 + s ROD + \frac{OD}{C}}$$

Error Transfer

Simplified Model while in Phase-Lock



Simplified Model while in Phase-Lock



Jitter Tolerance

SONET OC-48 Jitter Specifications

Tolerance 50 to 80% eye closure \longrightarrow want bandwidth high
0.15UI at baud/2500

Transfer 0.1dB peak \longrightarrow want bandwidth low
max bw = baud/1250

Generation 0.01UI_{rms} \longrightarrow want bandwidth high
0.1UI_{pp} or
low phase noise VCO

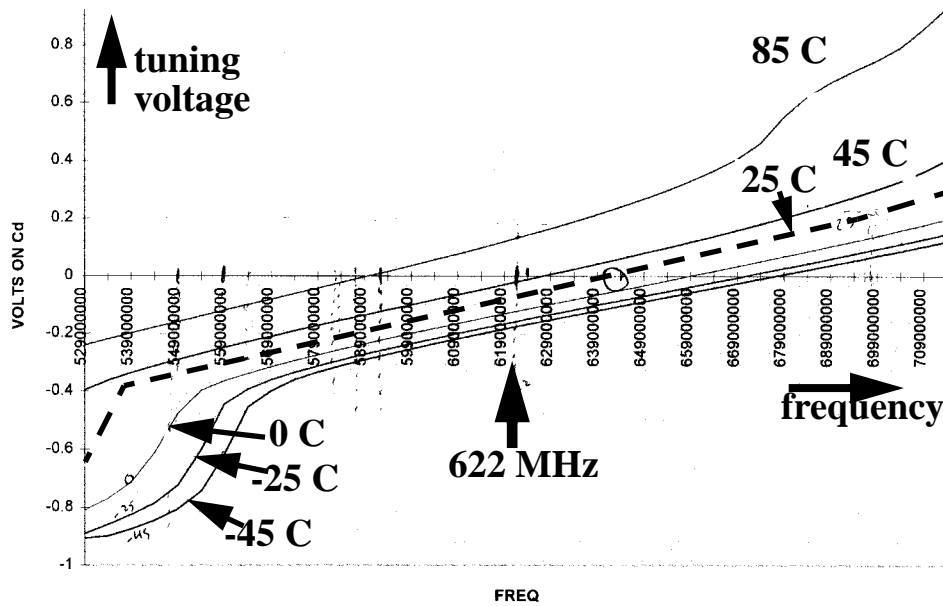
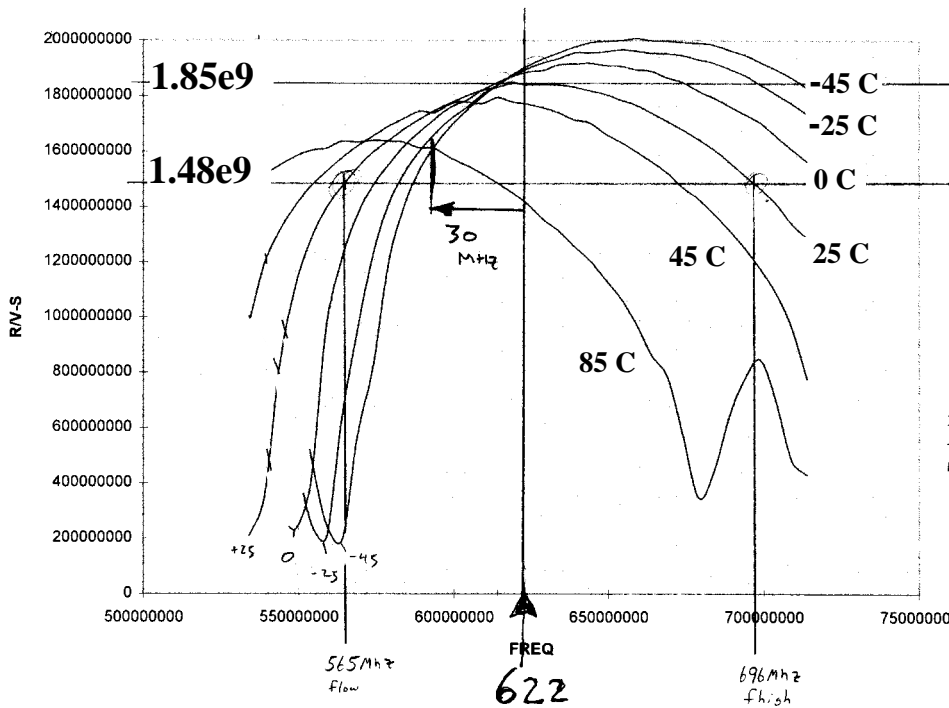
❄️ **nasty trade-off between tolerance and transfer**

❄️ **nasty tradeoff between generation and transfer**

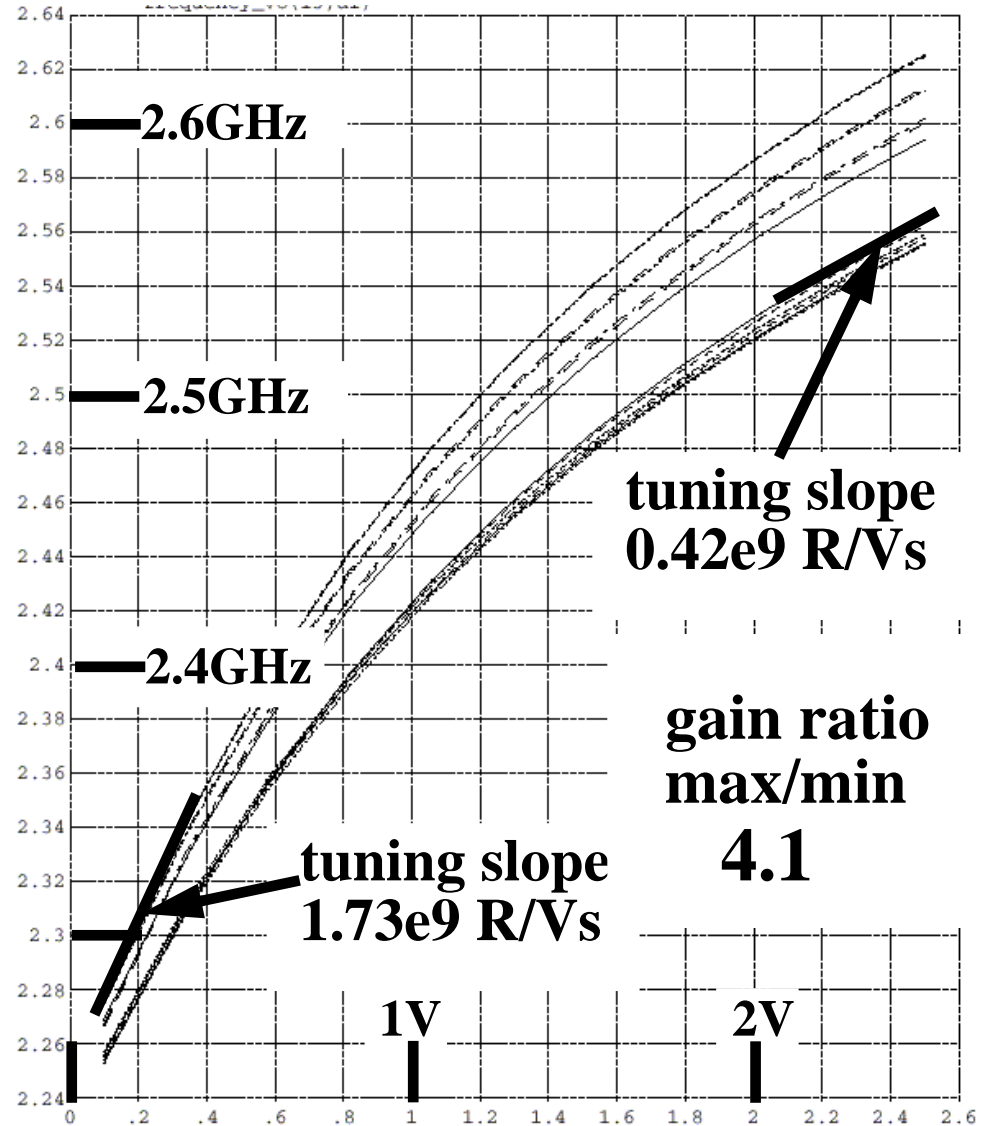
Conclusion: must control jitter bandwidth

Ring Oscillator VCO Gain

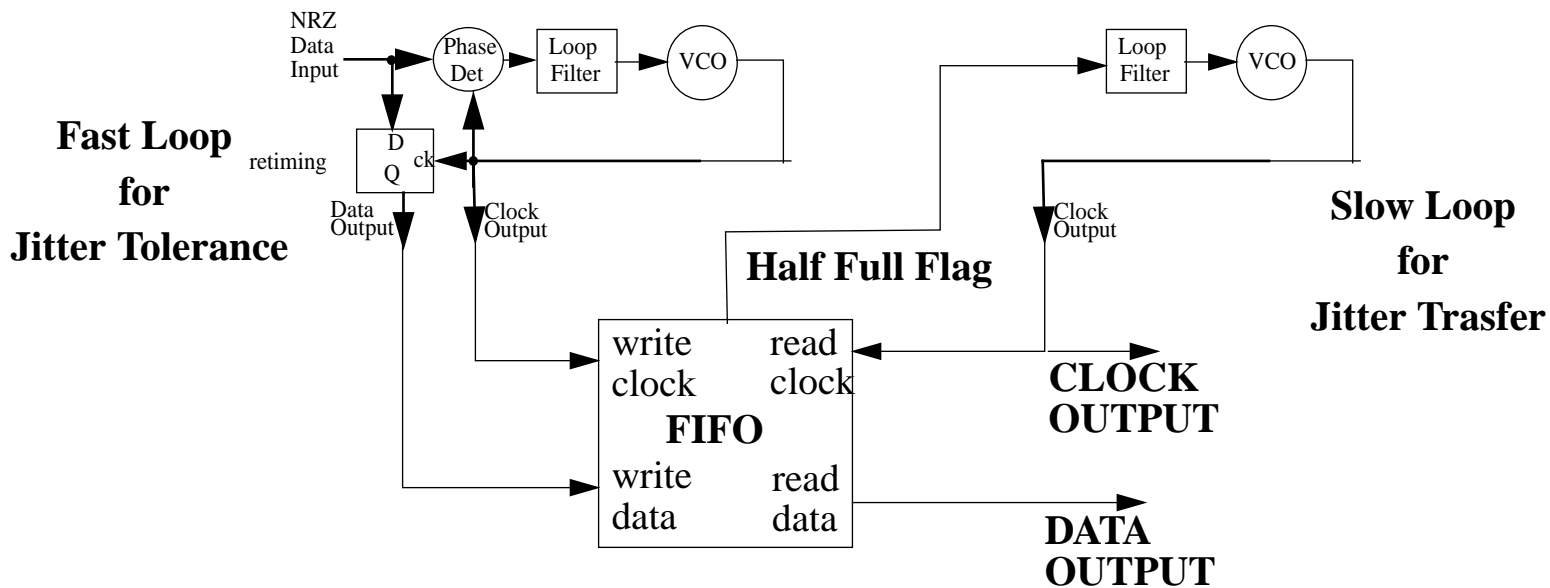
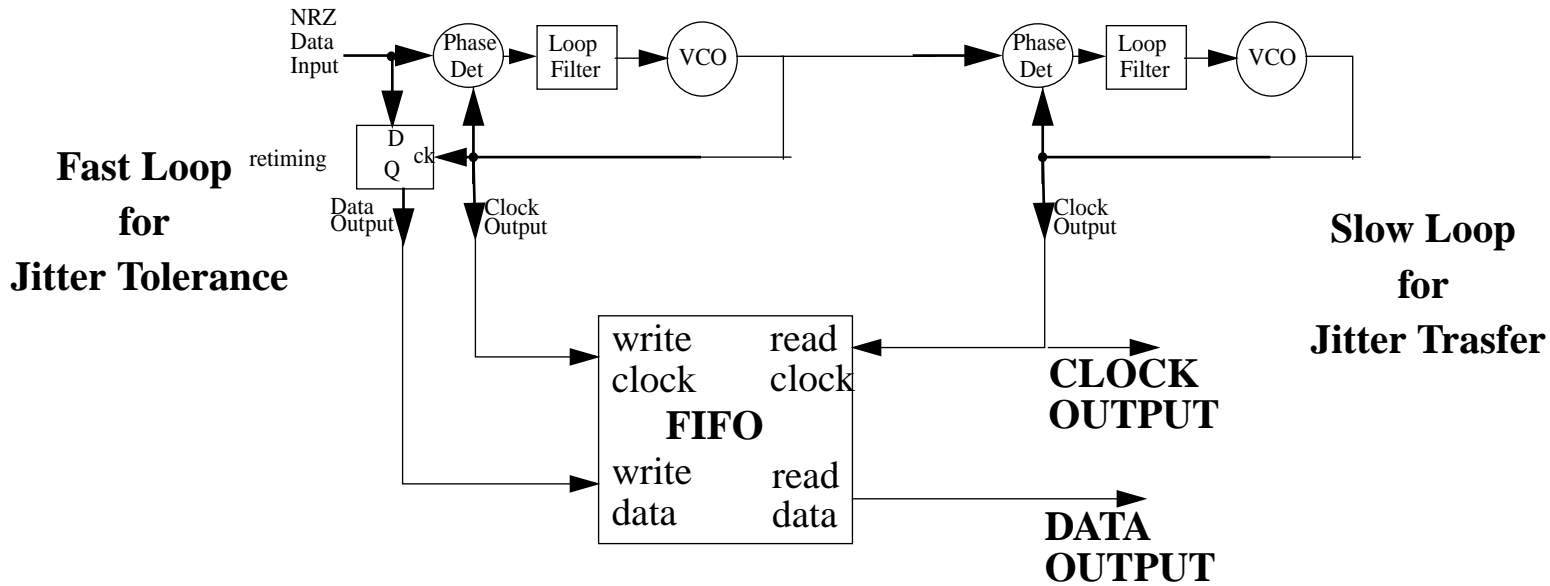
VCO GAIN SN#1



LC Oscillator VCO Gain

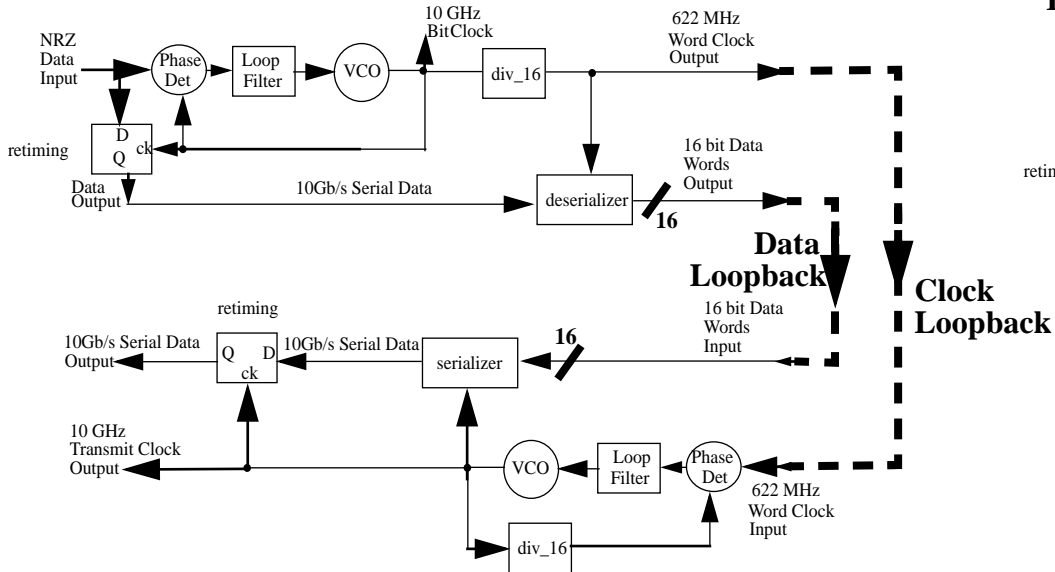


SONET Regenerator: two loops



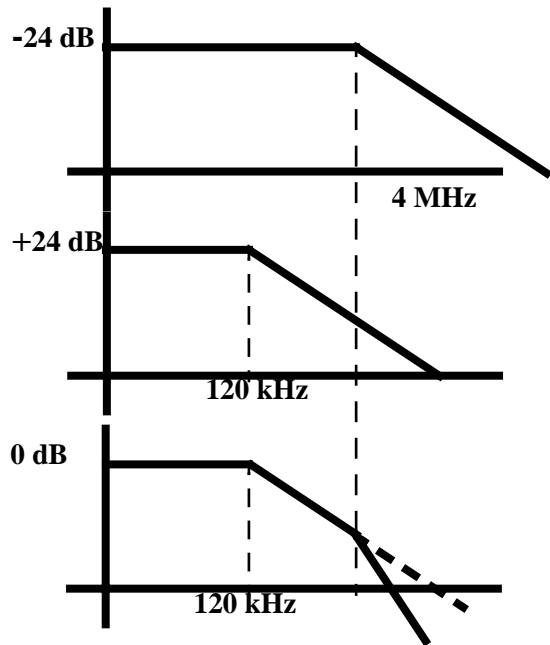
SONET Regenerator for OC-192

Fast Loop for Jitter Tolerance



Really Slow Loop for Jitter Transfer: 120 kHz ? I don't think so!
10GHz VCO is most fearsome: need -80dBc/Hz @ 120kHz offset

SONET Regenerator for OC-192



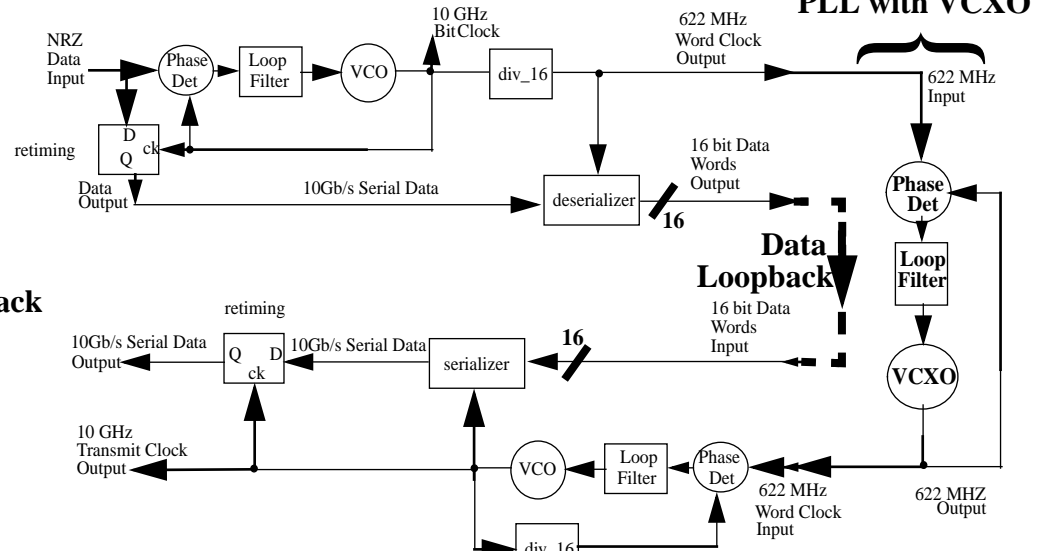
Receive Clock Recovery with div_16

Transmit Synthesizer Clock Multiplier Unit (CMU) times_16

Combined Jitter Transfer

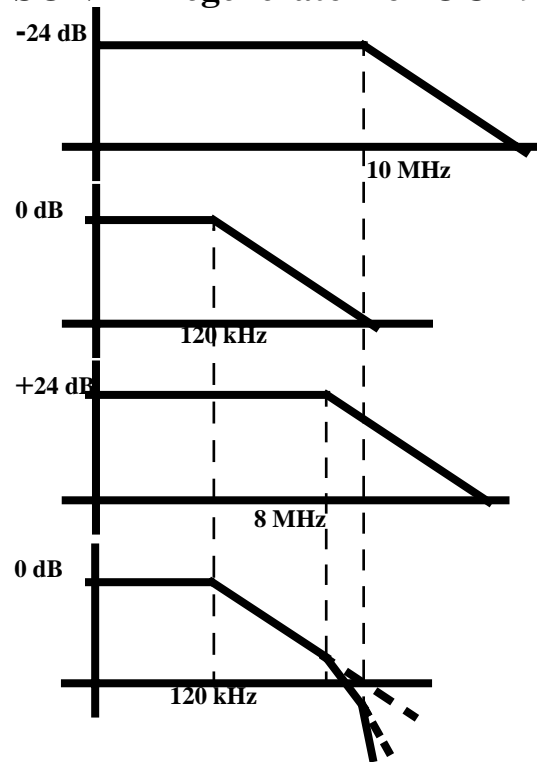
SONET Regenerator for OC-192

Fast Loop for Jitter Tolerance



Fast Loop to beat back VCO jitter

SONET Regenerator for OC-192



Receive Clock Recovery with div_16

Jitter Clean-Up PLL with VCXO

Transmit Synthesizer Clock Multiplier Unit (CMU) times_16

Combined Jitter Transfer

Delay- and Phase-Locked Loop

A 155-MHz Clock Recovery Delay- and Phase-Locked Loop

Thomas H. Lee, *Member, IEEE*, and John F. Bulzacchelli, *Student Member, IEEE*

IEEE JSSC vol. SC-27, pp.1736-1746, Dec 1992

Abstract—This paper describes a completely monolithic delay-locked loop (DLL) that may be used either by itself as a deskewing element, or in conjunction with an external voltage-controlled crystal oscillator (VCXO) to form a delay- and phase-locked loop (D/PLL). By phase shifting the input data rather than the clock, the DLL and D/PLL provide jitter-free clock recovery. Additionally, the jitter transfer function of the D/PLL has a low bandwidth for good jitter filtering without compromising acquisition speed. The D/PLL described here exhibits less than 1° rms jitter on the recovered clock, independent of the input data density. No jitter peaking is observed over the 40-kHz jitter bandwidth.

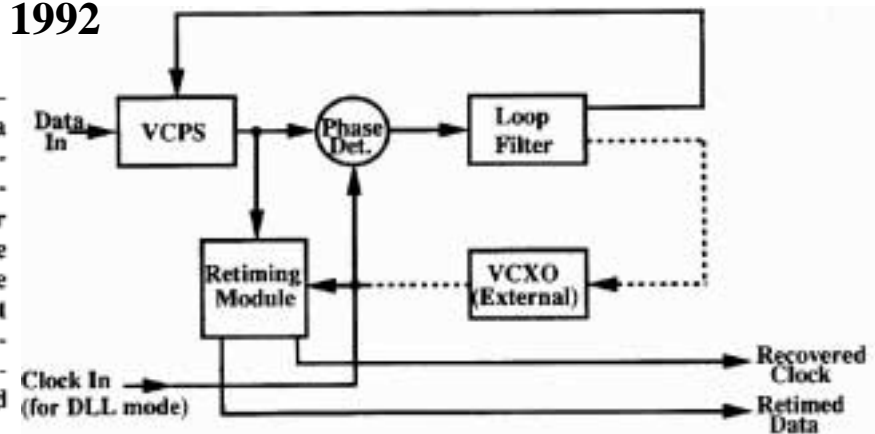
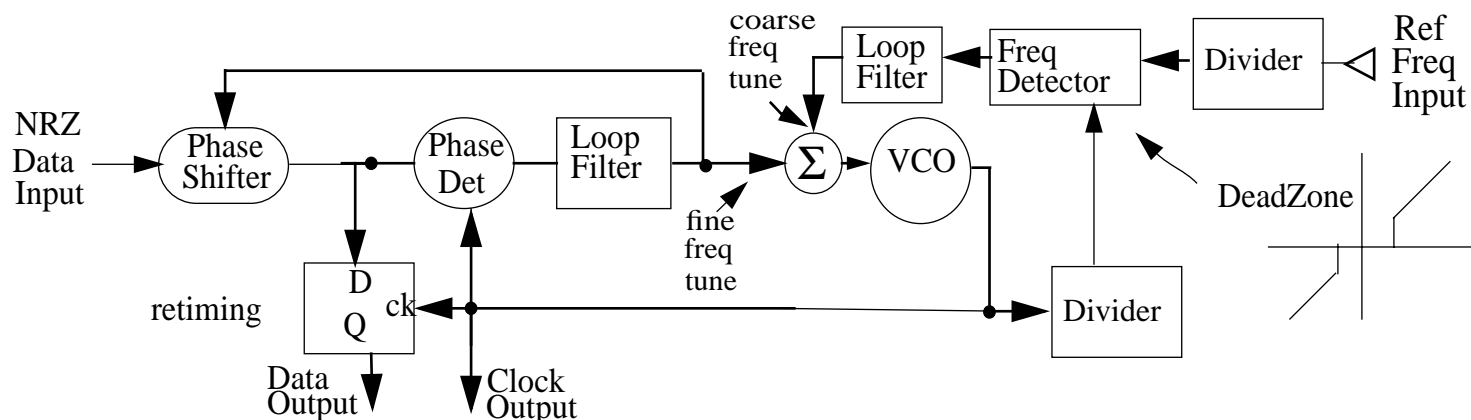
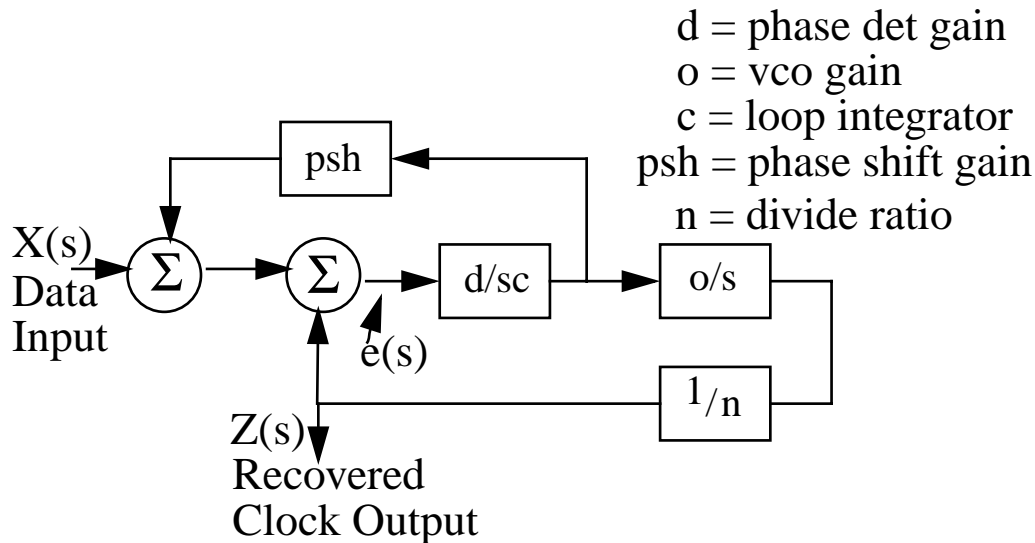


Fig. 7. Block diagram of DLL and D/PLL.



Delay- and Phase-Locked Loop

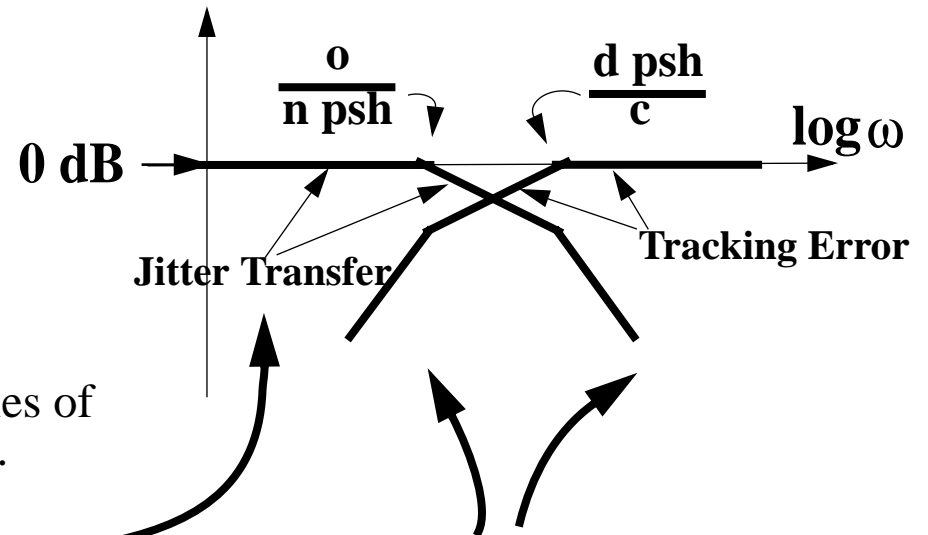
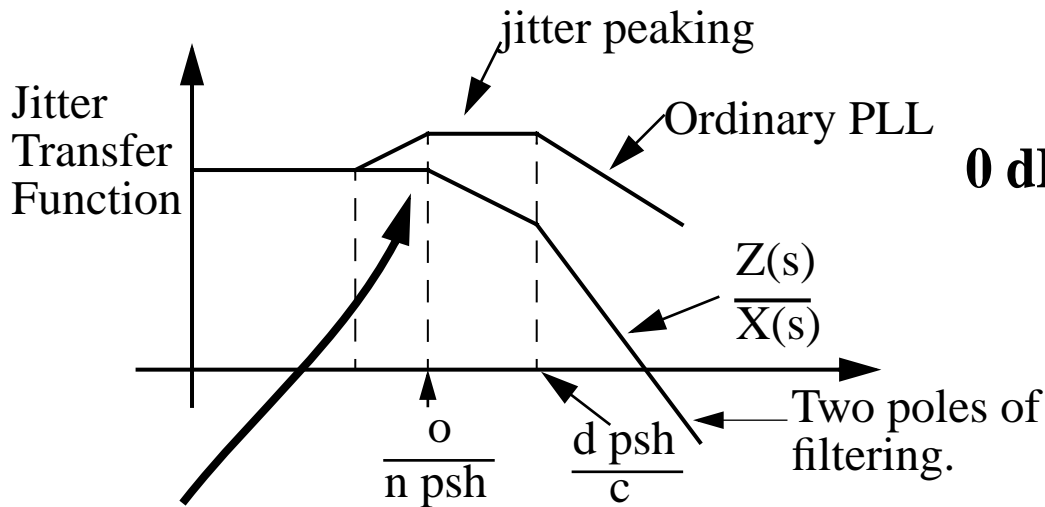


$$\frac{Z(s)}{X(s)} = \frac{1}{s^2 \frac{c n}{d o} + s \frac{n psh}{o} + 1}$$

Jitter Transfer Function

$$\frac{e(s)}{X(s)} = \frac{s^2}{s^2 + s \frac{d psh}{c} + \frac{d o}{c n}}$$

Tracking Error Transfer



No Jitter Peaking !!!

No tradeoff between Transfer and Tolerance !

Delay- and Phase-Locked Loop

THEORY OF OPERATION

The Delay- and Phase-Locked loop circuit for clock recovery and data retiming from an NRZ encoded data stream. The phase of the input data signal is tracked by two separate feedback loops which share a common control voltage. A high speed delay-locked loop path uses a voltage controlled phase shifter to track the high frequency components of input jitter. A separate frequency control loop comprising the vco tracks the low frequency components of input jitter. The initial frequency of the vco is set by yet a third loop which compares the vco frequency with an external reference frequency and sets the coarse tuning voltage. The jitter tracking phase-locked loop controls the vco by the fine tuning control.

The delay- and phase- loops together track the phase of the input data signal. For example, when the clock lags data, the phase detector drives the vco to higher frequency, and also, increases the delay through the phase shifter: these actions both serve to reduce the phase error between the clock and data. The faster clock picks up phase while the delayed data loses phase. Since the loop filter is an integrator, the static phase error will be driven to zero.

Another view of the circuit is that the phase shifter implements the zero required for frequency compensation of a second order phase-locked loop, and this zero is placed in the feedback path and thus, does not appear in the closed-loop transfer function. Jitter peaking in an ordinary second order phase-locked loop is caused by the presence of this zero in the closed-loop transfer function. Since this circuit has no zero in the closed-loop transfer, the jitter transfer function is completely free of jitter peaking.

The delay- and phase- loops together simultaneously provide wide-band jitter accommodation and narrow-band jitter filtering. The linearized block diagram in Figure 4 shows the jitter transfer function, $Z(s)/X(s)$, is a second order low pass providing excellent filtering. Note the jitter transfer has no zero, unlike an ordinary second order phase-locked loop. This means the circuit has fundamentally no jitter peaking, see Figure 5. Complete absence of peaking makes this circuit ideal for signal regenerator applications where jitter peaking in a cascade of regenerators can contribute to hazardous jitter accumulation.

The error transfer, $e(s)/X(s)$, has the same high pass form as an ordinary phase-locked loop. This transfer function is free to be optimized to give excellent wide-

Delay- and Phase-Locked Loop

band jitter accommodation since the jitter transfer function, $Z(s)/X(s)$, provides the narrow-band jitter filtering.

The delay- and phase- loops contribute to overall jitter accommodation. At low frequencies of input jitter on the data signal, the integrator in the loop filter provides high gain to track large jitter amplitudes with small phase error. In this case the vco is frequency modulated and jitter is tracked as in an ordinary phase-locked loop. The amount of low frequency jitter that can be tracked is a function of the vco tuning range. A wider tuning range gives larger accommodation of low frequency jitter. The internal loop control voltage remains small for small phase errors, so the phase shifter remains close to the center of its range and thus contributes little to the low frequency jitter accommodation.

At medium jitter frequencies, the gain and tuning range of the vco are not large enough to track input jitter. In this case the vco control voltage becomes large and saturates and the vco frequency dwells at one or the other extreme of its tuning range. The size of the vco tuning range, therefore has only a small effect on the jitter accommodation. The delay-locked loop control voltage is now larger, and so the phase shifter

takes on the burden of tracking the input jitter. The phase shifter range, in UI, can be seen as a broad plateau on the jitter tolerance curve. The phase shifter has a minimum range of $2UI$ at all data rates.

The gain of the loop integrator is small for high jitter frequencies, so that larger phase differences are needed to make the loop control voltage big enough to tune the range of the phase shifter. Large phase errors at high jitter frequencies cannot be tolerated. In this region the gain of the integrator determines the jitter accommodation. Since the gain of the loop integrator declines linearly with frequency, jitter accommodation is lower with higher jitter frequency. At the highest frequencies, the loop gain is very small, and little tuning of the phase shifter can be expected. In this case, jitter accommodation is determined by the eye opening of the input data, the static phase error, and the residual loop jitter generation. The jitter accommodation is roughly $0.5UI$ in this region. The corner frequency between the declining slope and the flat region is the closed loop bandwidth of the delay-locked loop, which is roughly $3MHz$.

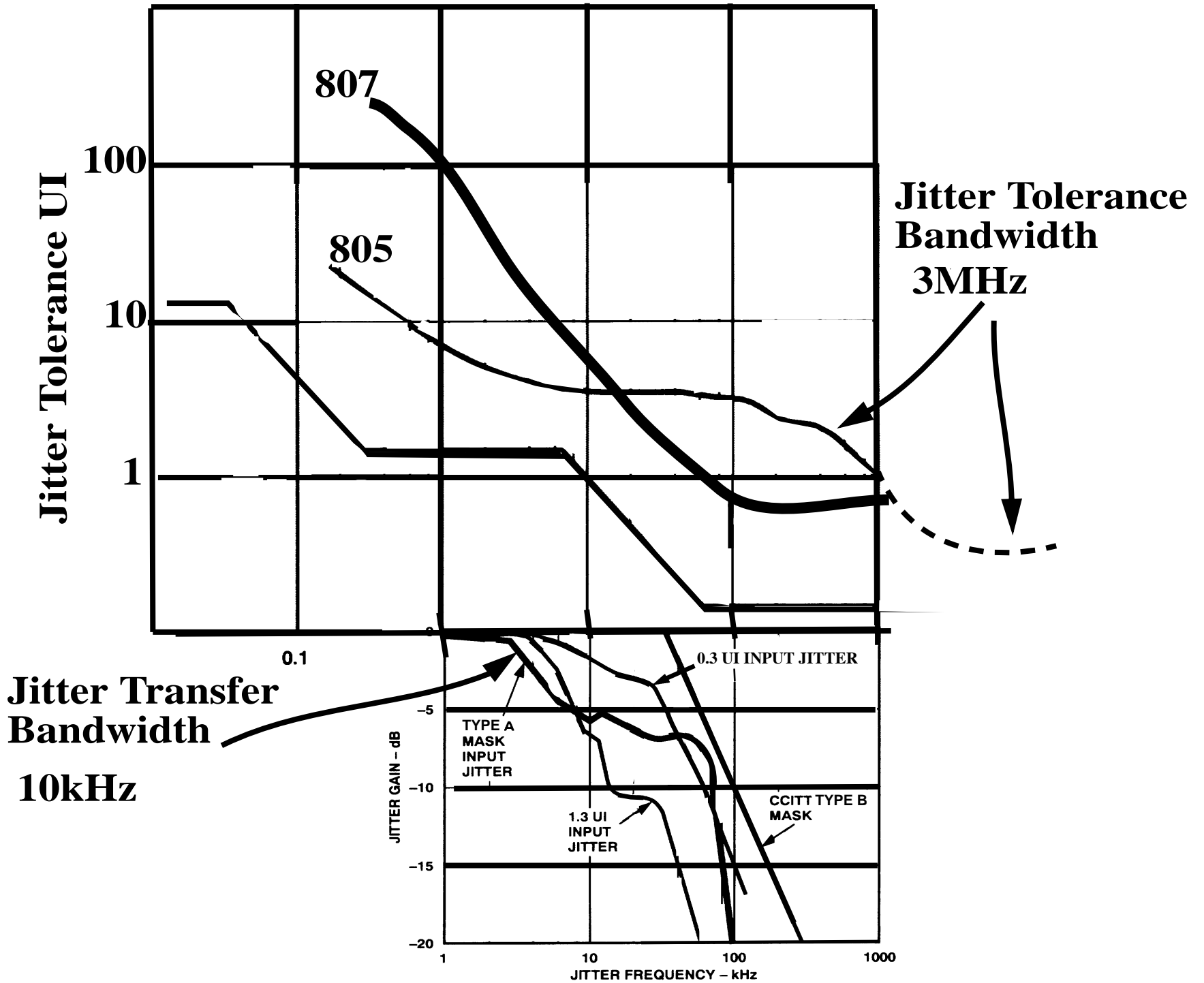


Figure 3. Jitter Transfer - Bandwidth

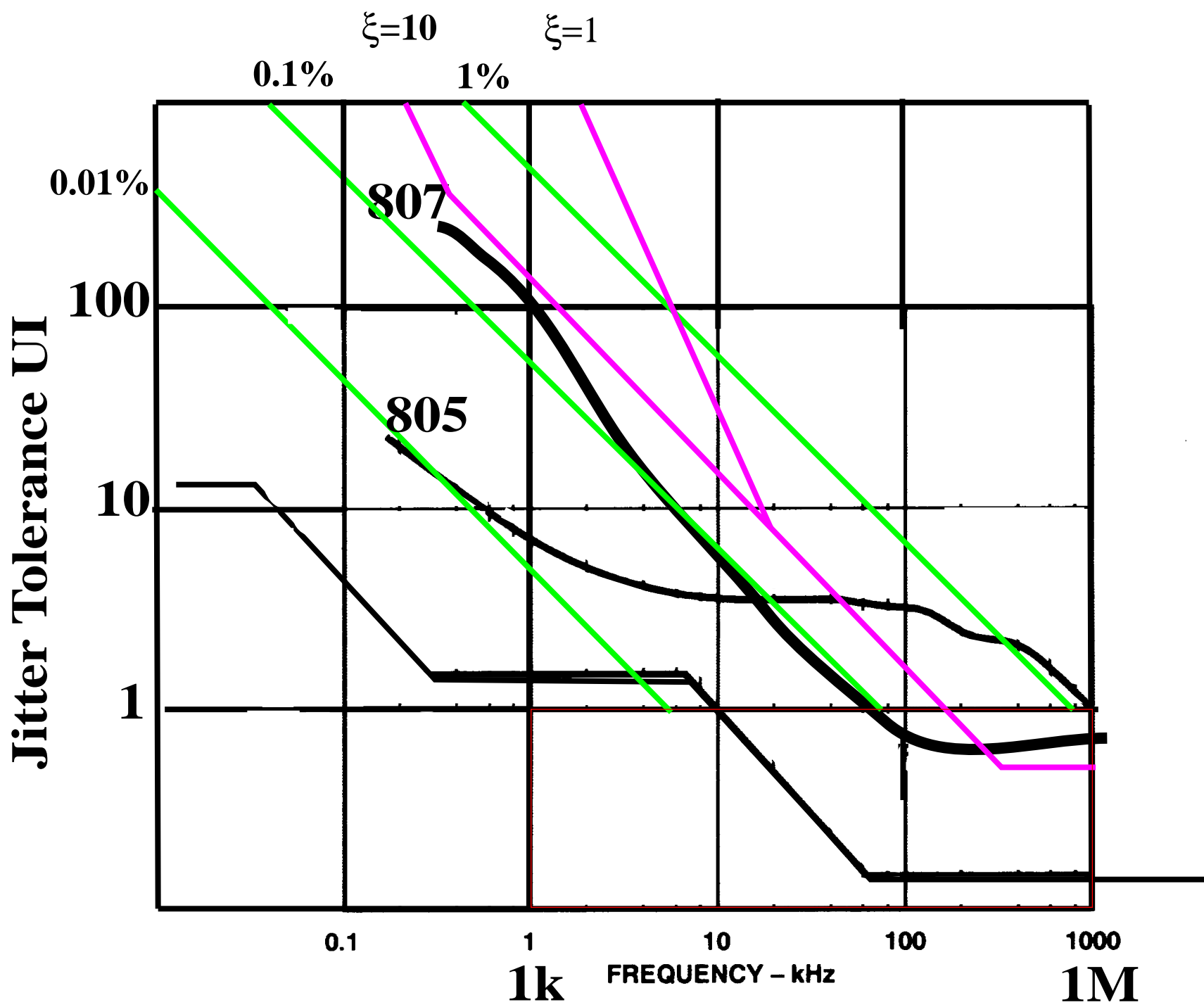
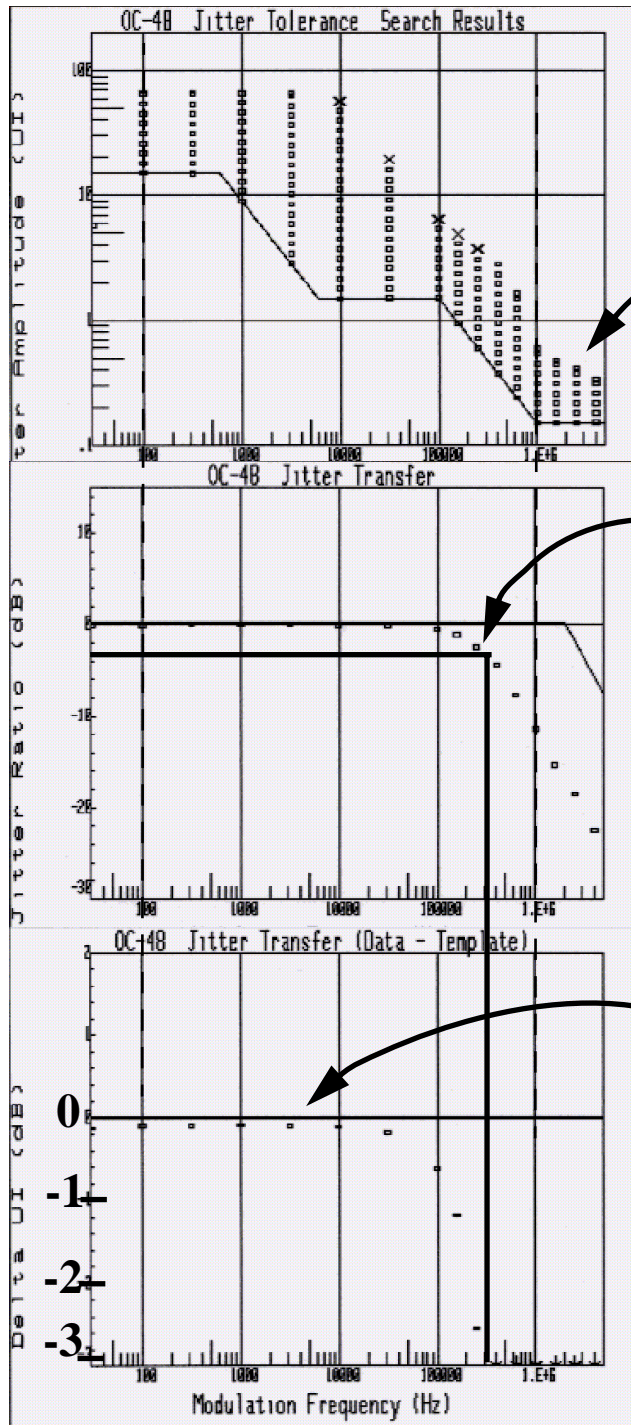


Figure 5. Jitter Tolerance

Delay- and Phase-Locked Loop: Results



**Jitter Tracking Bandwidth
3MHz**

**Jitter Transfer Bandwidth
300kHz**

Jitter Peaking Nil

Rate	Jitter Transfer				Jitter Tolerance		
	SONET Spec.	ADN2809 Implementation	Mask Corner Frequency	SONET Spec.	ADN2809 Implementation	Margin*	
OC3	130KHz	25.5KHz	65KHz	0.15UI _{pp}	1.0 UI _{pp}	6.67	
OC12	500KHz	80KHz	250KHz	0.15UI _{pp}	1.0 UI _{pp}	6.67	
OC48	2MHz	400KHz	1MHz	0.15UI _{pp}	1.0 UI _{pp}	6.67	

*Jitter Tolerance Data Limited by Test Equipment Capabilities

Table 1. Typical Jitter Transfer and Jitter Tolerance Performance

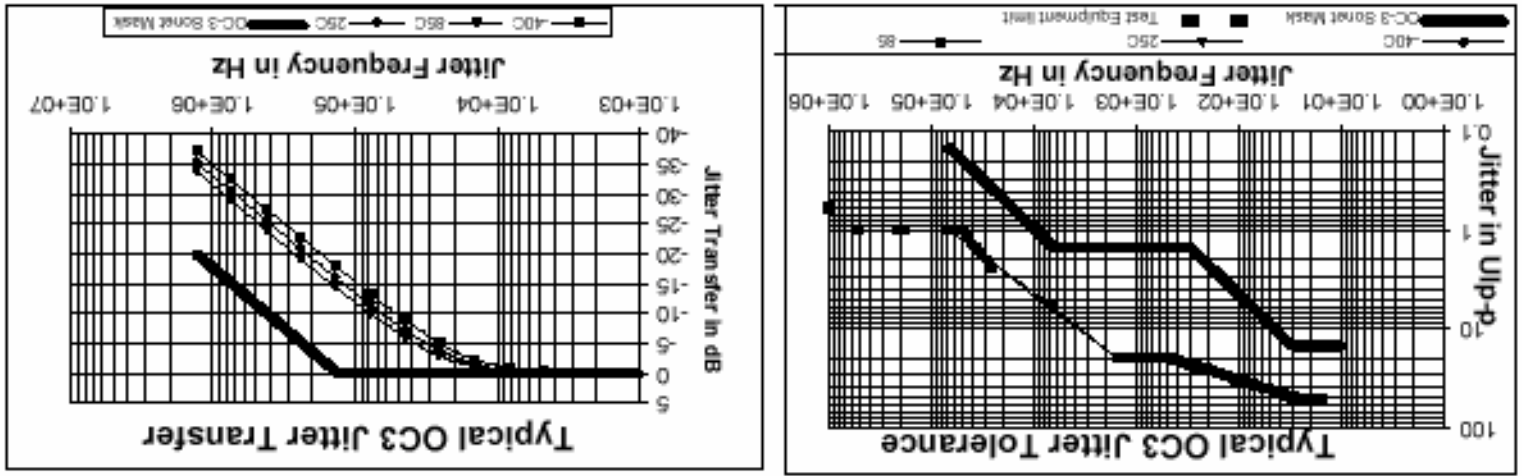
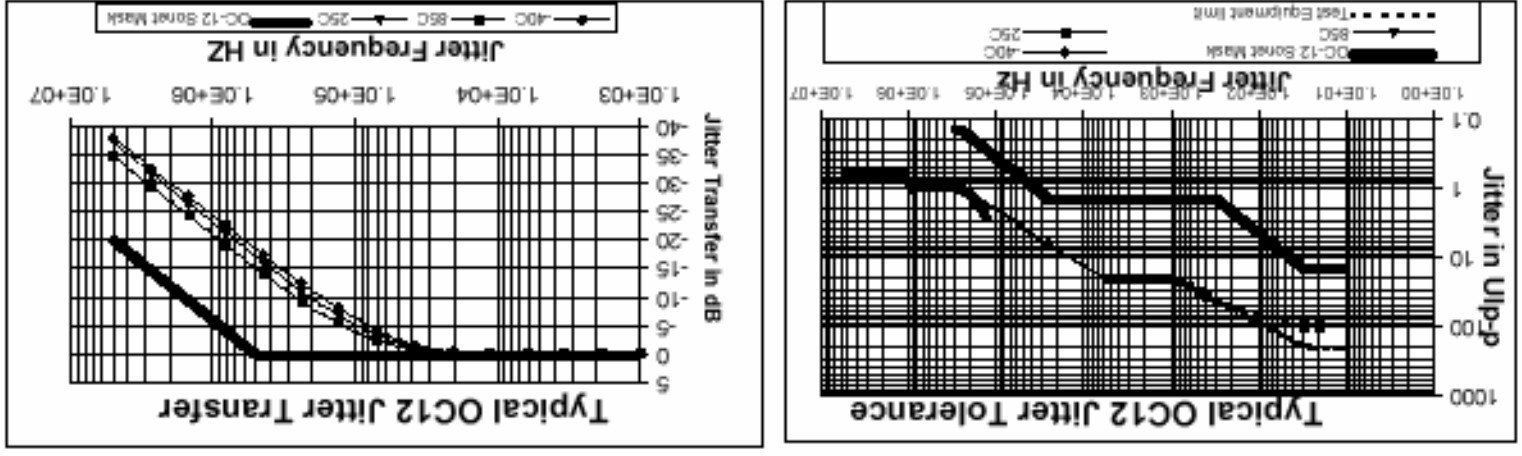
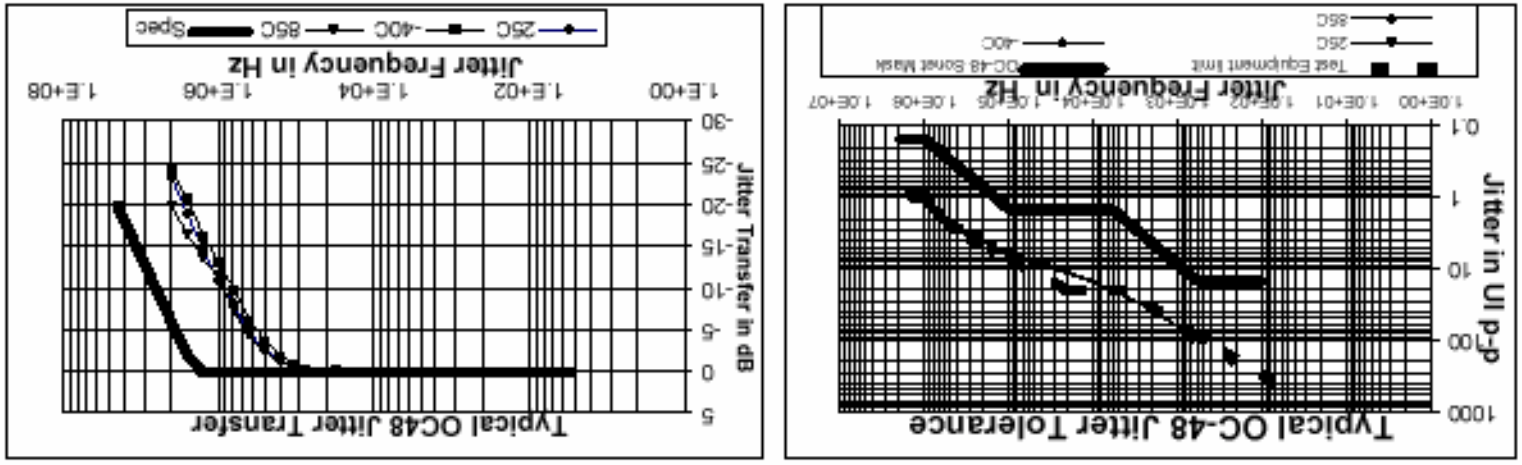
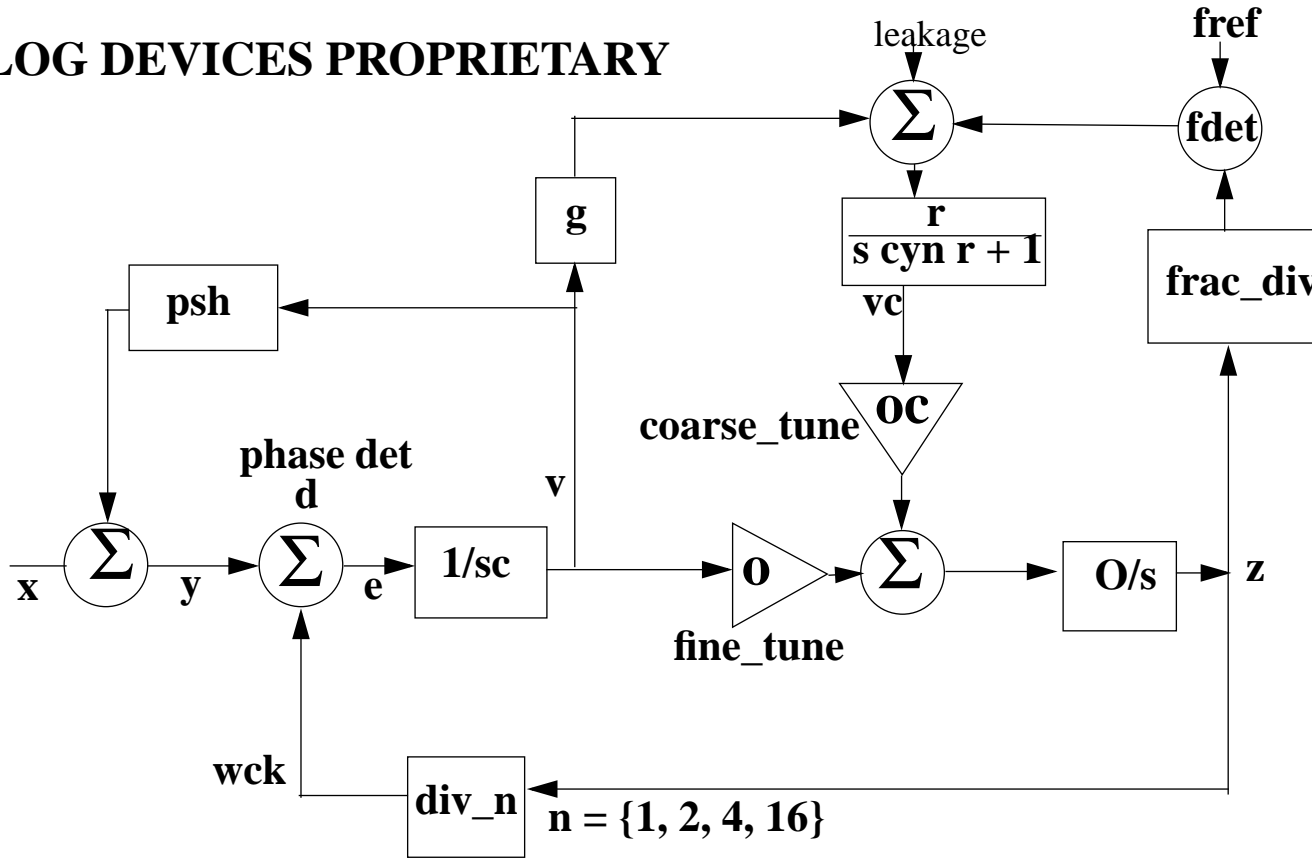


Figure 5. Jitter Tolerance and Transfer Bandwidth

ANALOG DEVICES PROPRIETARY



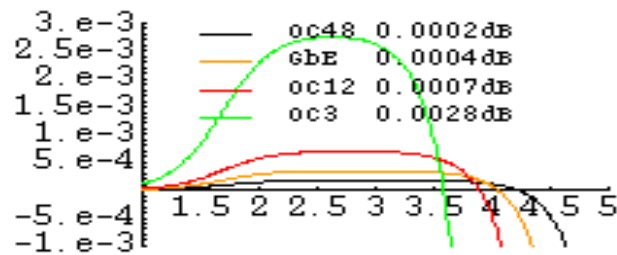
$$oco = \frac{oc}{o}$$

$$jpaprx = \frac{1 - \left(\frac{g}{cyn}\right) \left(\frac{n \text{ psh}}{o}\right) oco}{1 - 2 \left(\frac{g}{cyn}\right) \left(\frac{n \text{ psh}}{o}\right) oco}$$

$$jpaprx\tau = \frac{1 - oco \left(\frac{\tau_{tran}}{\tau_{synth}}\right)}{1 - 2 oco \left(\frac{\tau_{tran}}{\tau_{synth}}\right)}$$

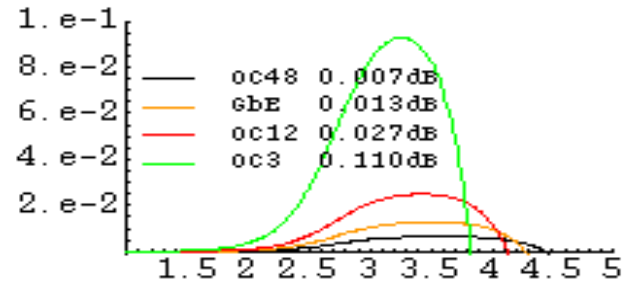
Jitter Peaking

ANALOG DEVICES PROPRIETARY



$d = 20. \text{e-}6$ $\text{psh} = 60.$
 $c = 40. \text{e-}12$
 $o = 140. \text{e}6$ $\text{oc} = 1.56 \text{e}9$
 $\text{cyn} = 4.7 \text{e-}6$ $g = 20. \text{e-}6$
 $r = 5. \text{e}6$

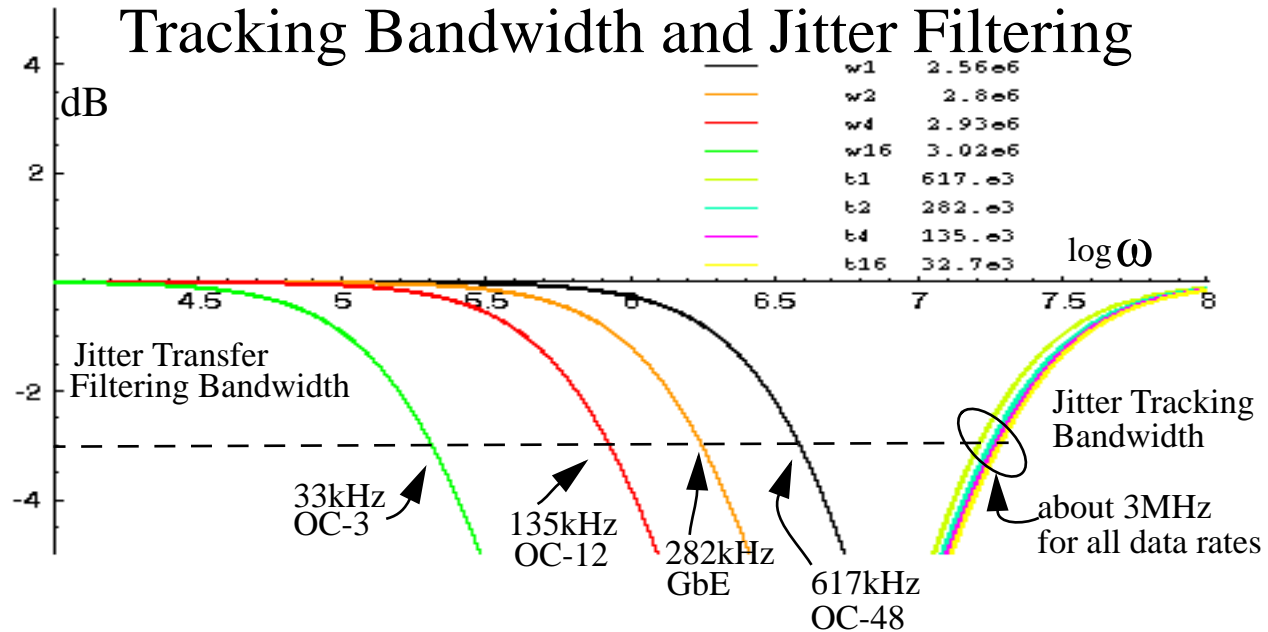
This is the nominal case. Note that everything at least a factor of 40 better than 0.1dB spec, even at OC-3 rate.



$d = 20. \text{e-}6$ $\text{psh} = 120.$
 $c = 40. \text{e-}12$
 $o = 82. \text{e}6$ $\text{oc} = 5. \text{e}9$
 $\text{cyn} = 3. \text{e-}6$ $g = 26. \text{e-}6$
 $r = 5. \text{e}6$

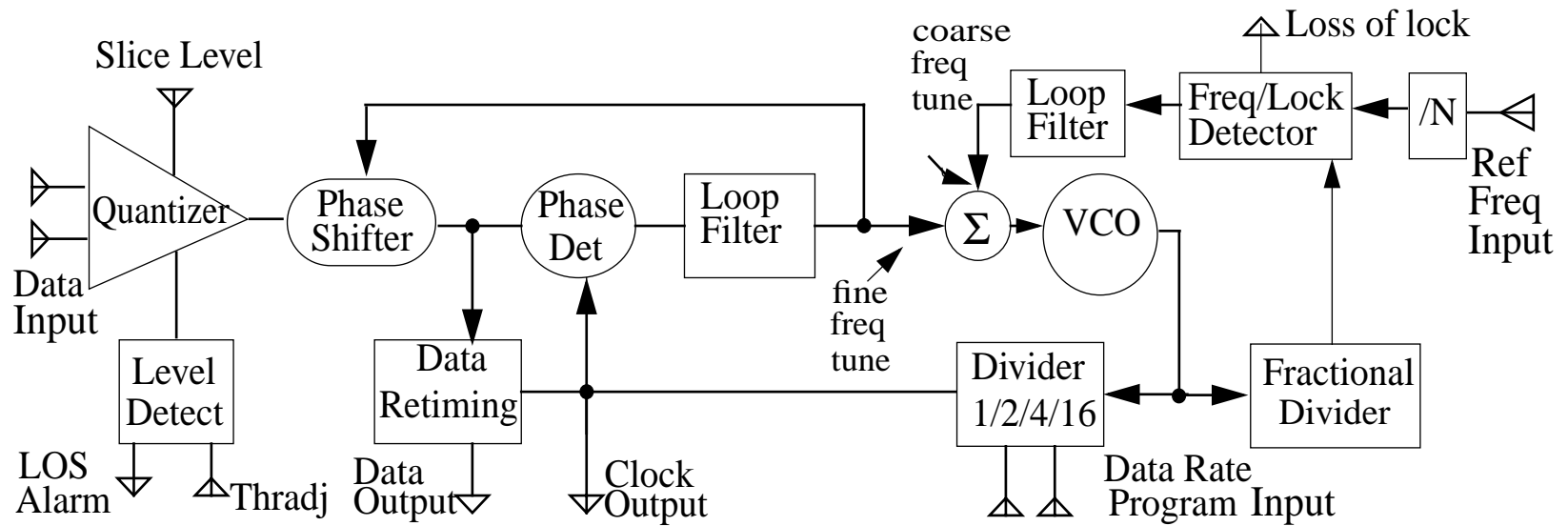
This is the worst case. Note the jitter peaking exceeds 0.1dB for the OC-3 rate.

FIGURE 3

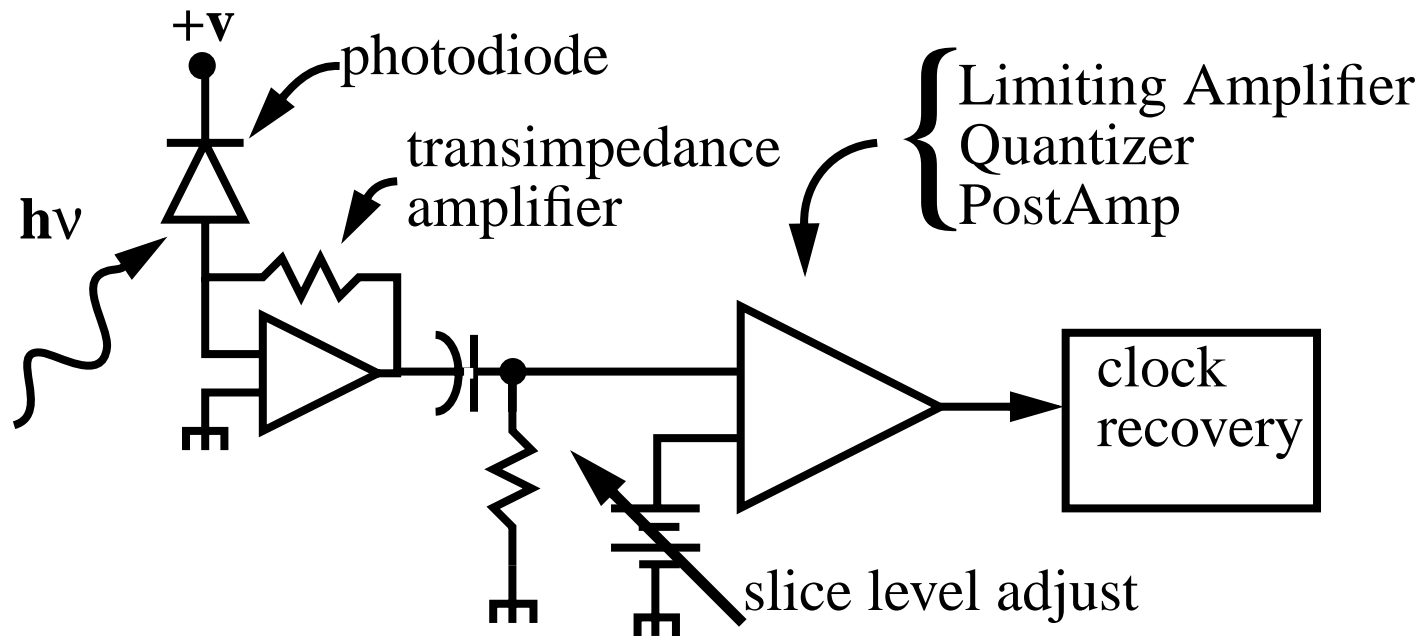


d = 16.e-6 c = 50.e-12 o = 195.e6 psh = 60.

FAST	Tol	Margin	SLOW	Tran	Margin
OC48					
2.56e6	1MHz	2.56	617.e3	2MHz	3.24
GbE					
2.8e6	500k	5.6	282.e3	1MHz	3.54
OC12					
2.93e6	250k	11.7	135.e3	500k	3.7
OC3					
3.02e6	65k	46.5	32.7e3	130k	3.98



Data Threshold



ADN2819

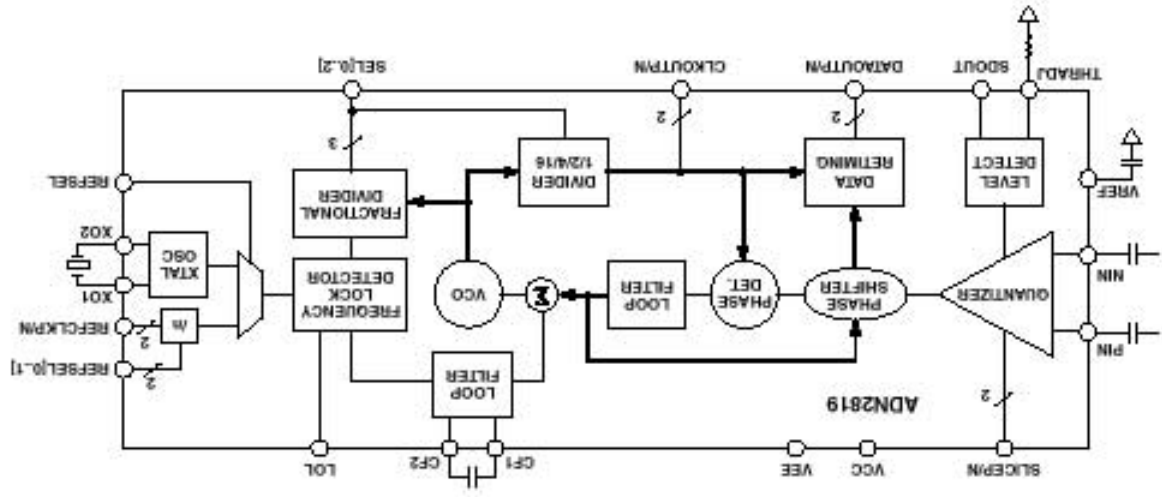
FEATURES

- Meets SONET Requirements for Jitter Transfer/Generation/Tolerance
- Quantizer Sensitivity: 4 mV Typ
- Adjustable Slice Level: ± 100 mV
- 1.9 GHz Minimum Bandwidth
- Patented Clock Recovery Architecture
- Loss of Signal Detect Range: 3 mV to 15 mV
- Single Reference Clock Frequency for All Rates, Including 15/14 (7%) Wrapper Rate
- Choice of 19.44 MHz, 38.88 MHz, 77.76 MHz, or 155.52 MHz
- REFCLK (LVPECL/LVDS/LVCMOS/LVTTL Compatible Inputs (LVPECL/LVDS Only at 155.52 MHz)
- 19.44 MHz Oscillator On-chip to Be Used with External Crystal
- Loss of Lock Indicator
- Loopback Mode for High Speed Test Data
- Output Squelch and Bypass Features
- Single-Supply Operation: 3.3 V
- Low Power: 540 mW Typical
- 7 mm x 7 mm 48-Lead LFCSP

APPLICATIONS

- SONET OC-3/-12/-48, SDH STM-1/-4/-16, GBE and 15/14 FEC Rates
- WDM Transponders
- Regenerators/Repeaters
- Test Equipment
- Backplane Applications

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The ADN2819 provides the receiver functions of quantization, signal level detect, and clock and data recovery at rates of OC-3, OC-12, OC-48, Gigabit Ethernet, and 15/14 FEC rates. All SONET jitter requirements are met, including jitter transfer, jitter generation, and jitter tolerance. All specifications are quoted for -40°C to $+85^{\circ}\text{C}$ ambient temperature, unless otherwise noted.

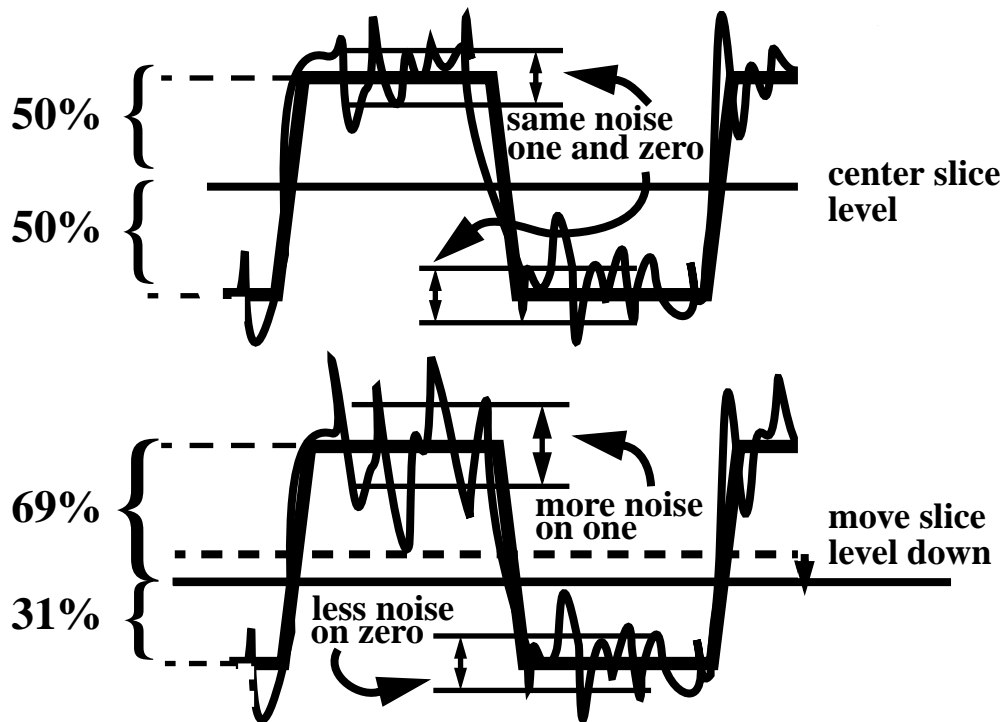
The device is intended for WDM system applications and can be used with either an external reference clock or an on-chip oscillator with external crystal. Both native rates and 15/14 rate digital wrappers are supported by the ADN2819, without any change of reference clock.

This device, together with a PIN diode and a TIA preamplifier, can implement a highly integrated, low cost, low power, fiber optic receiver.

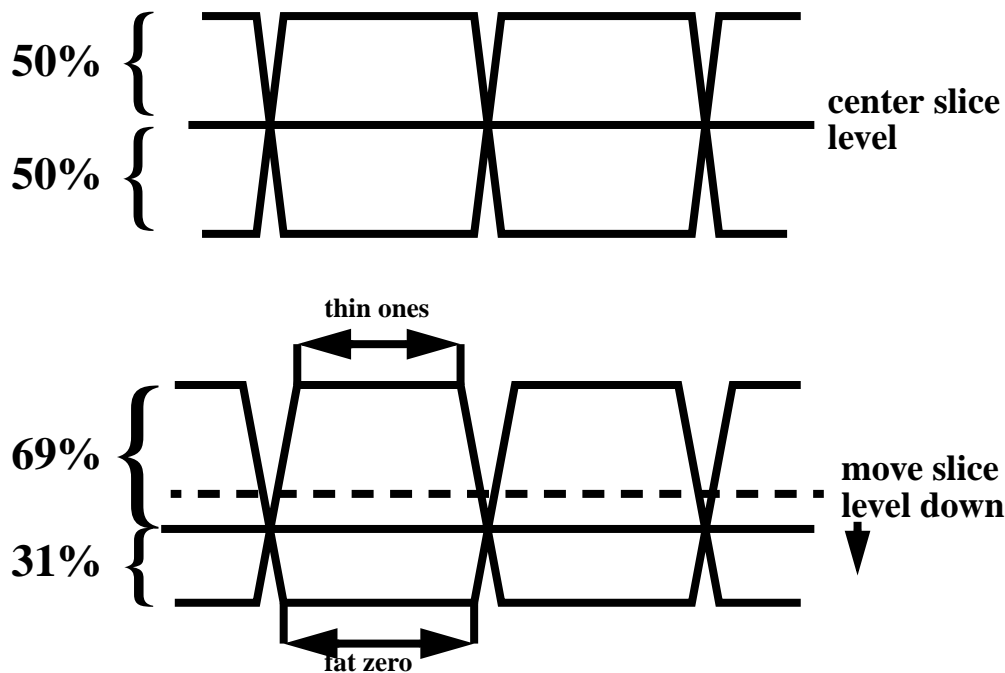
The receiver front end signal detect circuit indicates when the input signal level has fallen below a user-adjustable threshold. The signal detect circuit has hysteresis to prevent chatter at the output.

The ADN2819 is available in a compact 7 mm x 7 mm 48-lead chip-scale package.

Amplified Spontaneous Emission in Optical Amplifier



Eye Distortion in Optical Amplifier



Impaired Eye

