



90nm Technology Design Challenge

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May 10, 2004.

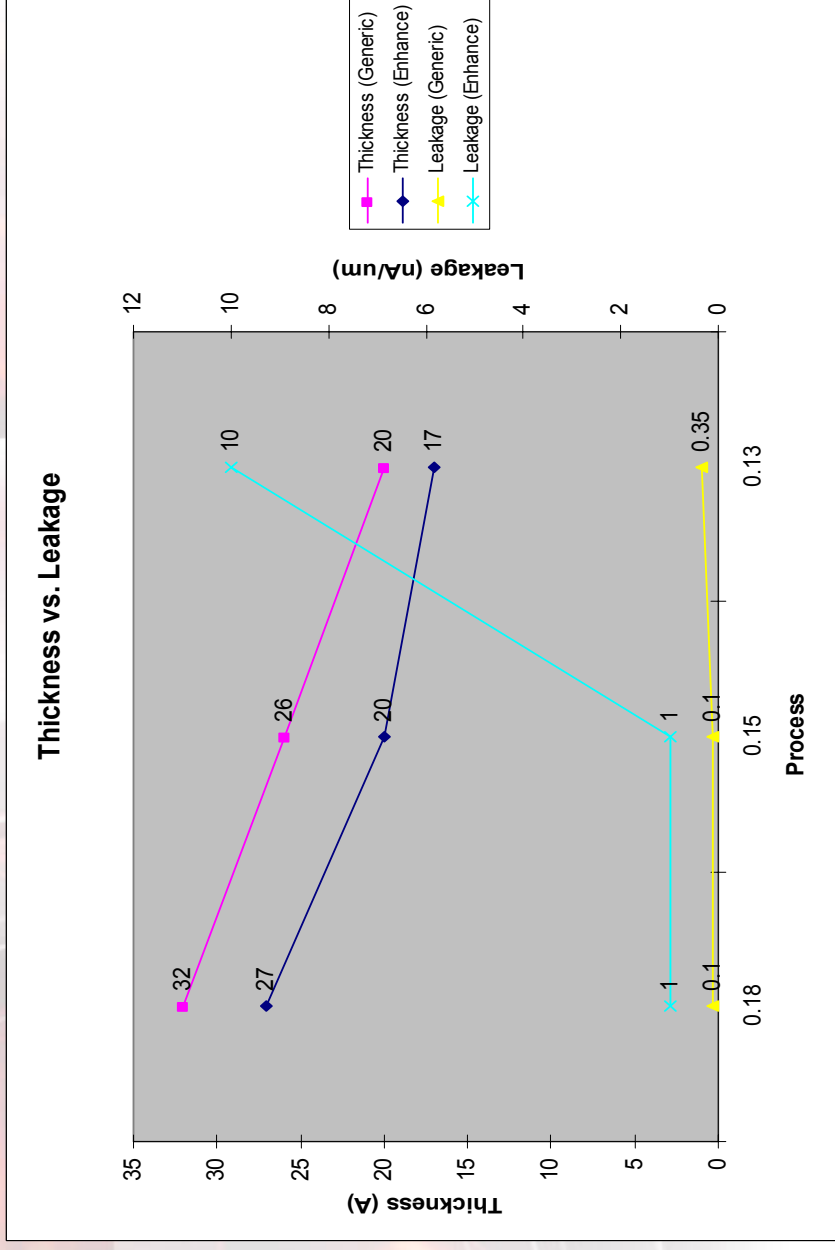
Overview

- Leakage Optimization
- Active Power Reduction
- Crosstalk
- Electromigration
- Stress Migration
- Inductance Impact
- Design For Manufacture
- Chip/Package Integration



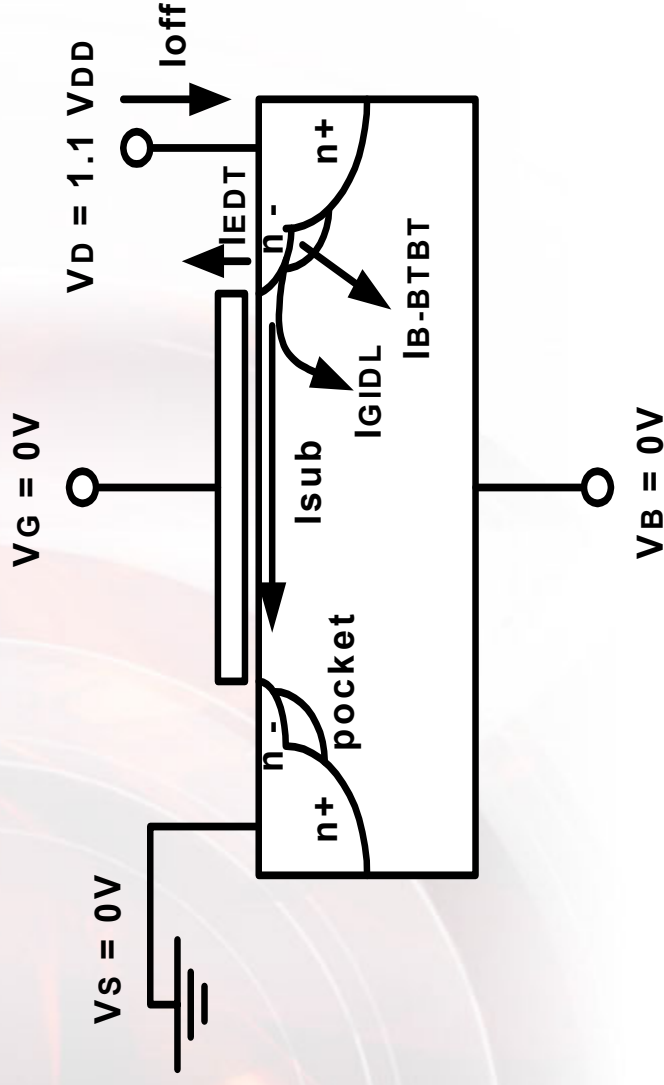
Leakage Trend

- Leakage is significantly increased for process because of small channel length and thinner gate oxide

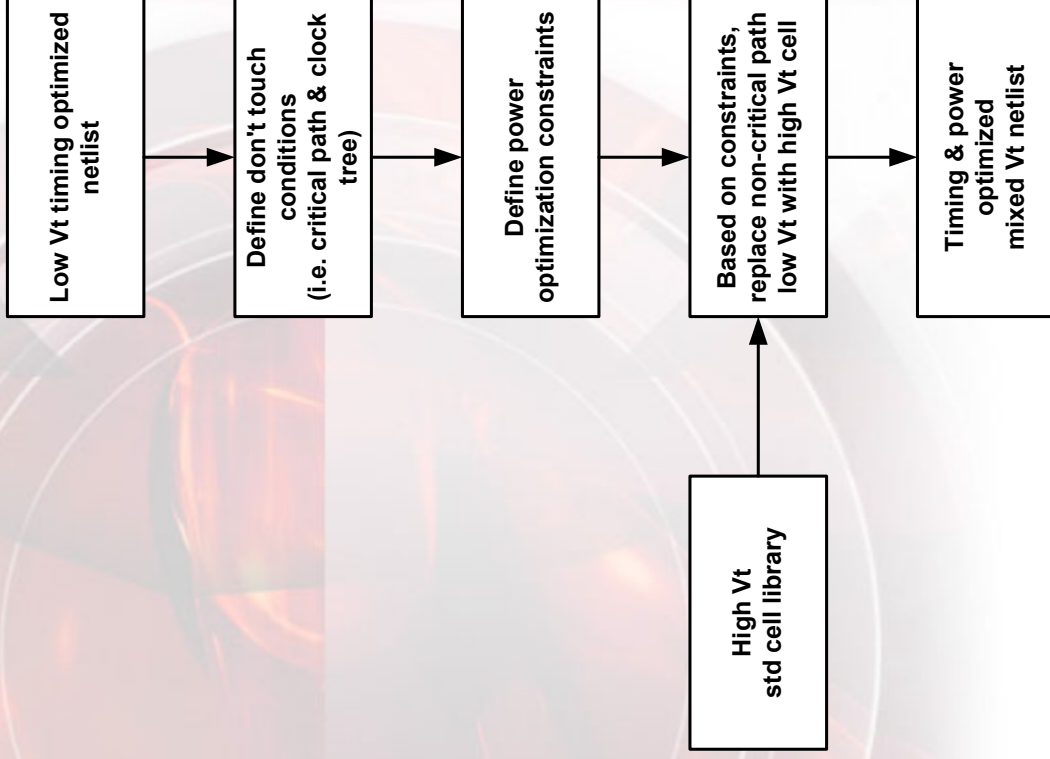


Leakage Source

- Due to device architecture change, both gate and subthreshold leakage becomes the major leakage source. The gate leakage is highly dependent on gate area and the subthreshold leakage is increased exponentially with temperature



Leakage Optimization



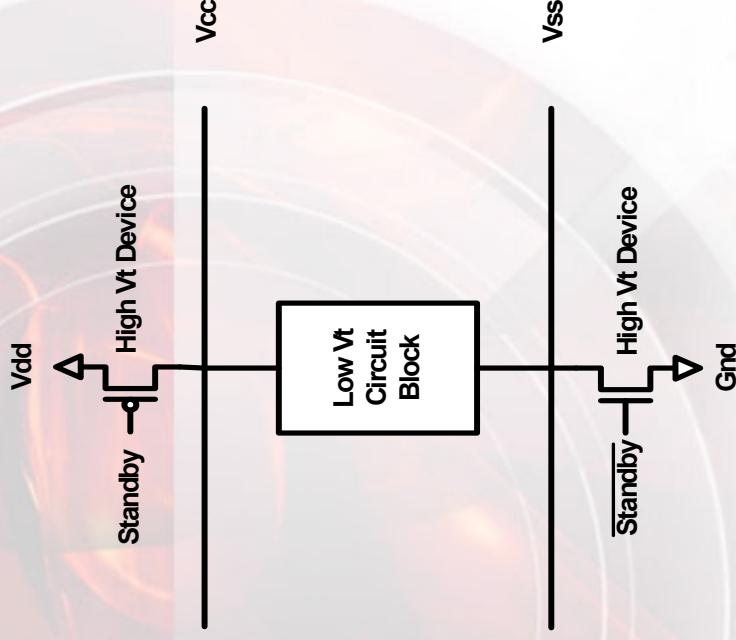
- Multiple Vt Flow
 - Integrate different Vt standard cells in same design for leakage reduction, however, it may not be sufficient for 90nm process because the high Vt device leakage is also high



Leakage Optimization

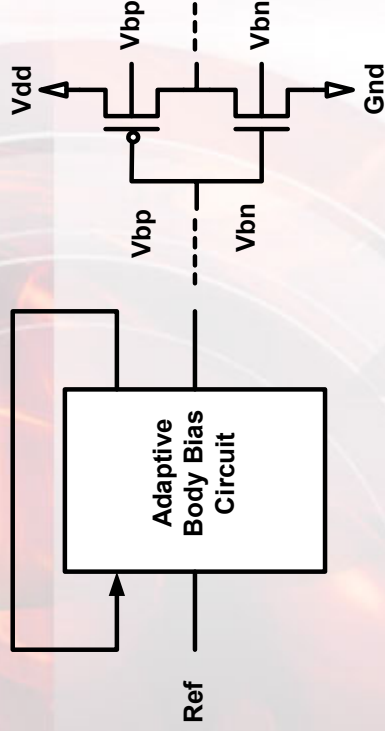


- Multiple Threshold CMOS (MTCMOS)
 - Apply the high V_t device as a sleep control to shut down the power during the standby mode
 - Modified flip flop is required to preserve the data during standby mode
 - Area penalty of large switch and modified flip flop prohibited this approach for general applications



Leakage Optimization

- Variable Threshold CMOS (VTCMOS)
 - Modify the standard cell to separate the body bias with power supply
 - Adaptive body bias circuit is required to control the bias voltage for leakage reduction
 - This approach can be used to minimize the process variation
 - Require triple well process for substrate isolation



Active Power Reduction

- Active Power
 - Since design complexity increases from generation to generation, more devices are integrated into single die, then, the overall power is increased dramatically due to gate count increase
 - The performance is improved in recent years, the operating frequency increases which results in significant power dissipation too. The side effect of large power dissipation is the temperature increase, it has negative impact toward the system design

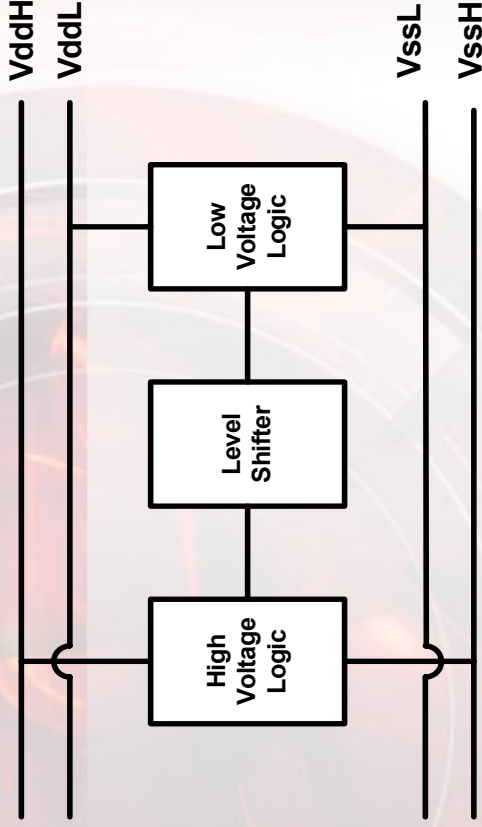


Active Power Reduction



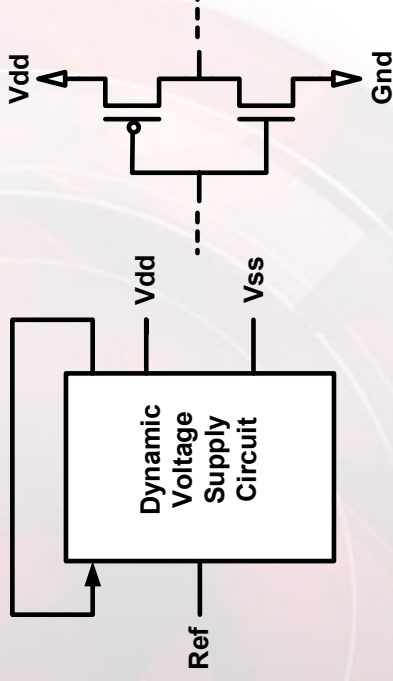
- Multiple Voltage Supply

- It is also called voltage island approach to reduce the supply voltage for power minimization
- To include additional low voltage supply for non-critical logic
- Additional level shifter is required to interface between logic with different supply voltages
- It complicates the overall power grid design with additional area penalty as well as the physical design flow



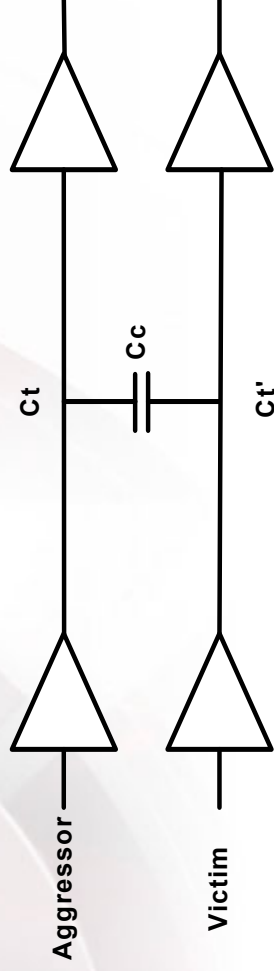
Active Power Reduction

- Dynamic Voltage Scale (DVS)
 - To vary the power supply/frequency dynamically for power reduction
 - Complex control dynamic voltage supply control scheme is required to regulate the voltage supply
 - The trade-off is the logic performance is significantly degraded



Crosstalk

- Crosstalk
 - For nanometer technology, the total capacitance is dominated by coupling capacitance, especially for minimum width/spacing metal wire. The cross coupling between adjacent wire becomes serious and has negative impact toward the timing analysis
 - Crosstalk is mainly dependent on several factors: drive strength, wire length/spacing, edge rate and propagation direction



Crosstalk

- Crosstalk Prevention
 - Buffer Insertion
 - To insert additional buffer, it breaks long RC chain and increases the victim net signal strength
 - Buffer Sizing
 - To increase buffer drive strength, it also minimize the aggressor impact toward victim net
 - Wire Spreading
 - To increase the spacing between two nets, it significantly reduces the coupling capacitance and minimize the crosstalk impact
 - Wire Shielding
 - To isolate the aggressor impact toward the victim through power/ground wire shielding



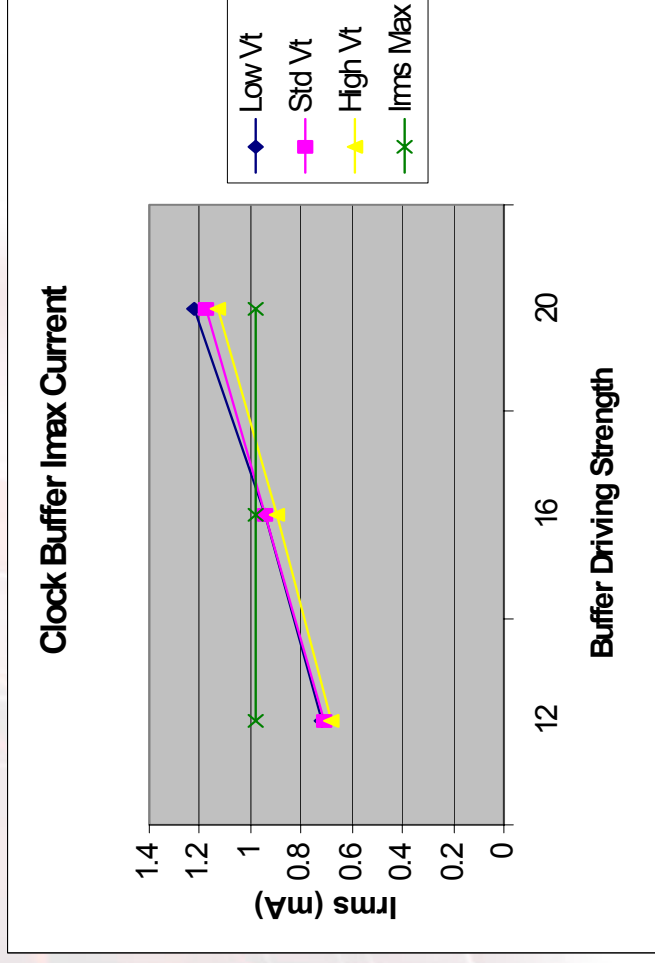
Electromigration

- Electromigration (EM)
- Electromigration is resulted from excess electrons flow through the wire for long period of time, it eventually causes short and open issues. Moreover, it is worse for unidirectional current rather than the bidirectional current.
- Electromigration is further divided into DC and AC EM, DC EM is related with power mesh design and AC EM is referred to signal propagation.
- Copper maximum current density is higher than aluminum one, however, the advantage diminished when the layout geometry is further shrunk
- For nanometer technology, the via current density is lower than metal wire, therefore, more via contacts are required for power supply connection. It becomes important for IP development and full chip power mesh design



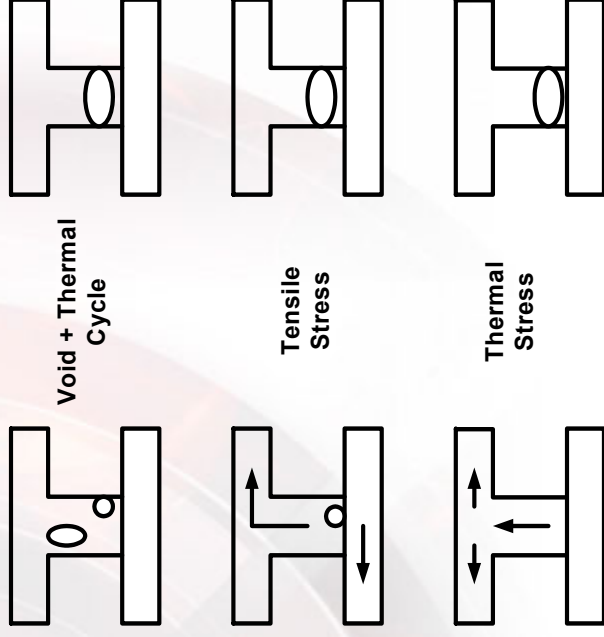
Electromigration

- The output current of high drive cell with low V_t device may easily exceed maximum current density limitation at AC mode, it often happens in clock tree design, then, the electromigration guideline is required for high drive cell usage



Stress Migration

- Stress Migration
 - Stress migration is referred to copper process and mainly related with several reasons: void formation, tensile stress and thermal stress
 - In order to prevent stress migration, it is recommended to insert more via in the wire to avoid the via open



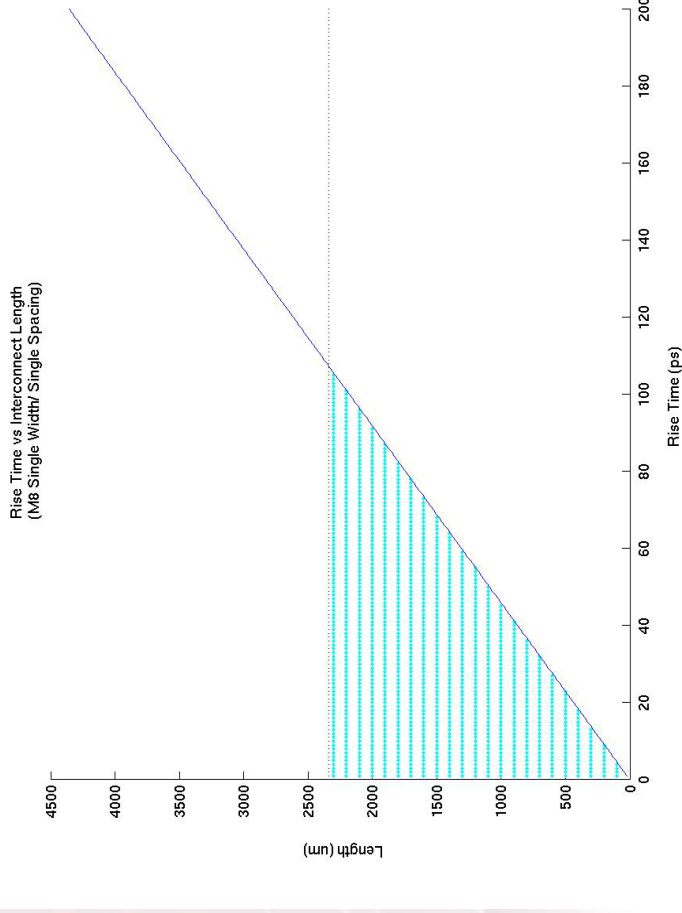
Inductance Impact

- Overview
 - There are two different type of inductance: self and mutual inductance: self inductance is dependant on the layout geometry but the mutual inductance is related with signal return path, the inductance is reduced at high frequency
 - The inductance increases total impedance value and results in less crosstalk interference



Inductance Impact

- Inductance becomes more important when the input edge rate is small with small RC constant thick metal line. It reduces the edge rate but increases the propagation delay then results in incorrect timing estimation. The effect is diminished for long metal line due to larger RC constant

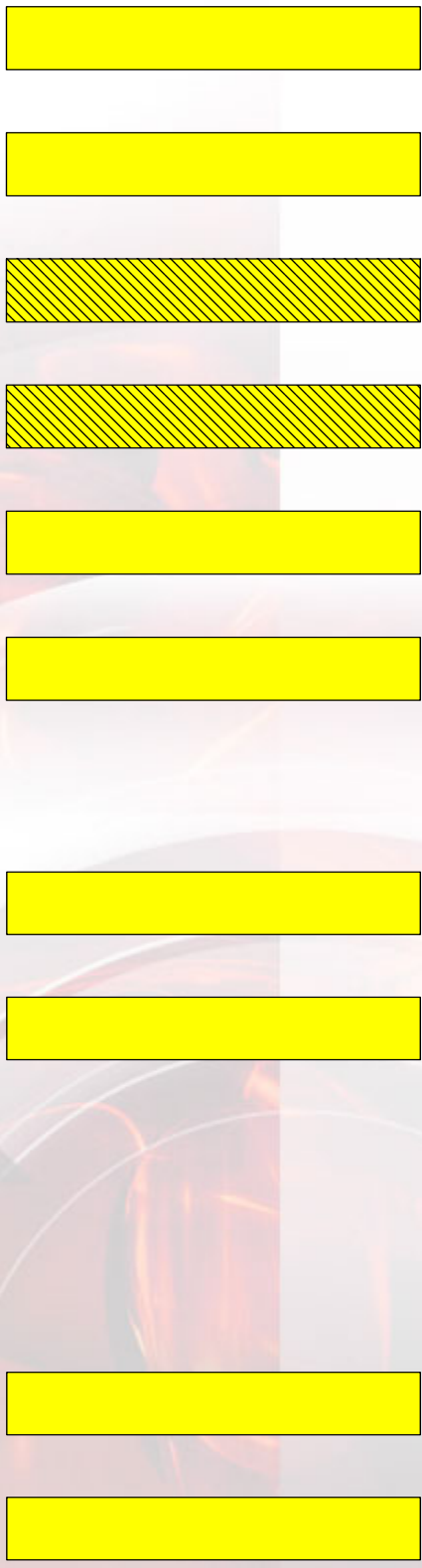


Design For Manufacture

- Process Variation
 - For nanometer technology, the design is subjected to layout due to small geometry size. It has direct impact toward the process variation and affect the device characteristics
 - For 300mm (12”) wafer migration, the wafer area is almost twice as 200mm (8”) one, it is difficult to control the consistent device parameters across the large area and results in significant yield and performance drawback



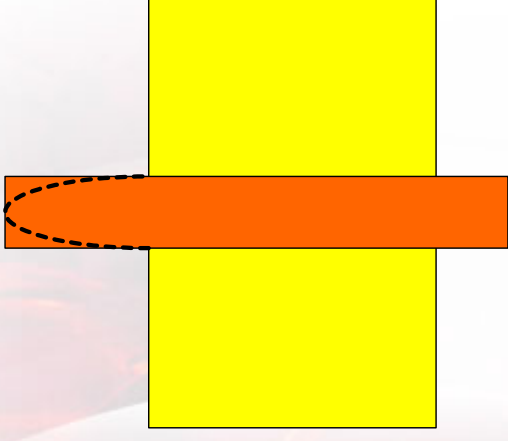
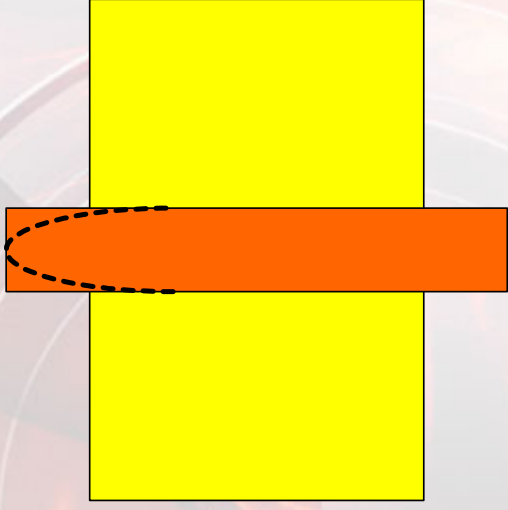
Design for Manufacture



- Non-uniform diffusion distribution, it affects the device characteristics
- Insert the dummy diffusion to maintain uniformity across the chip



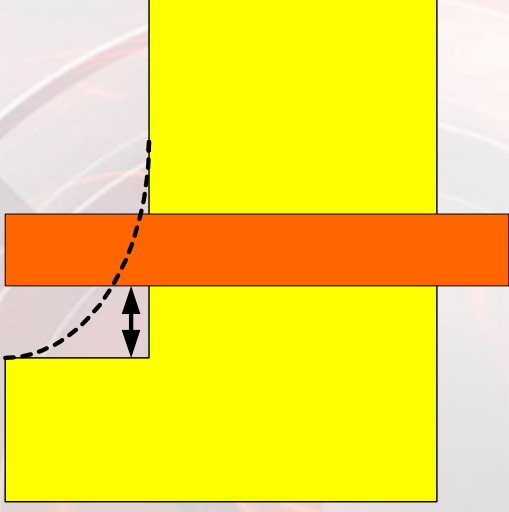
Design for Manufacture



- Minimum poly endcap causes the device threshold variation due to rounding effect, especially for small poly gate
- Increase poly endcap dimension



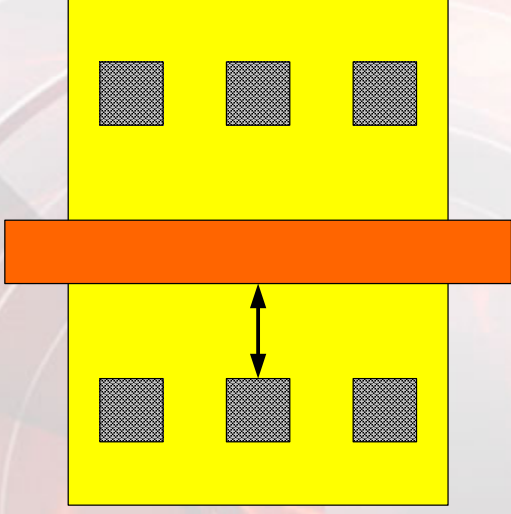
Design for Manufacture



- L-shape implant also causes the device threshold variation
- Increase L-shape implant to/overlap gate spacing to avoid the rounding effect



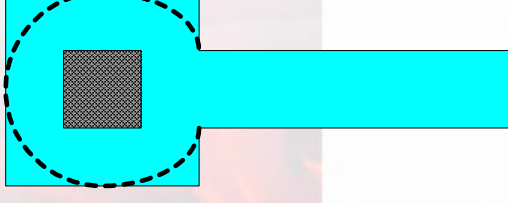
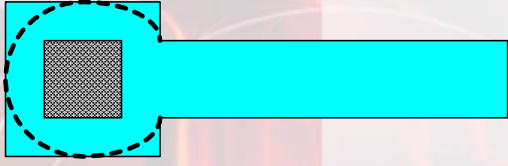
Design for Manufacture



- Minimum contact to poly gate spacing (especially for small poly gate) to cause the Idsat variation, the degradation becomes more serious for contact scare structure
- Increase the contact to poly gate spacing to minimize Idsat degradation



Design for Manufacture



- Minimum metal to contact enclosure easily cause the contact open during the mask making process
- Increase metal island size to enlarge the opening to avoid mask making failure



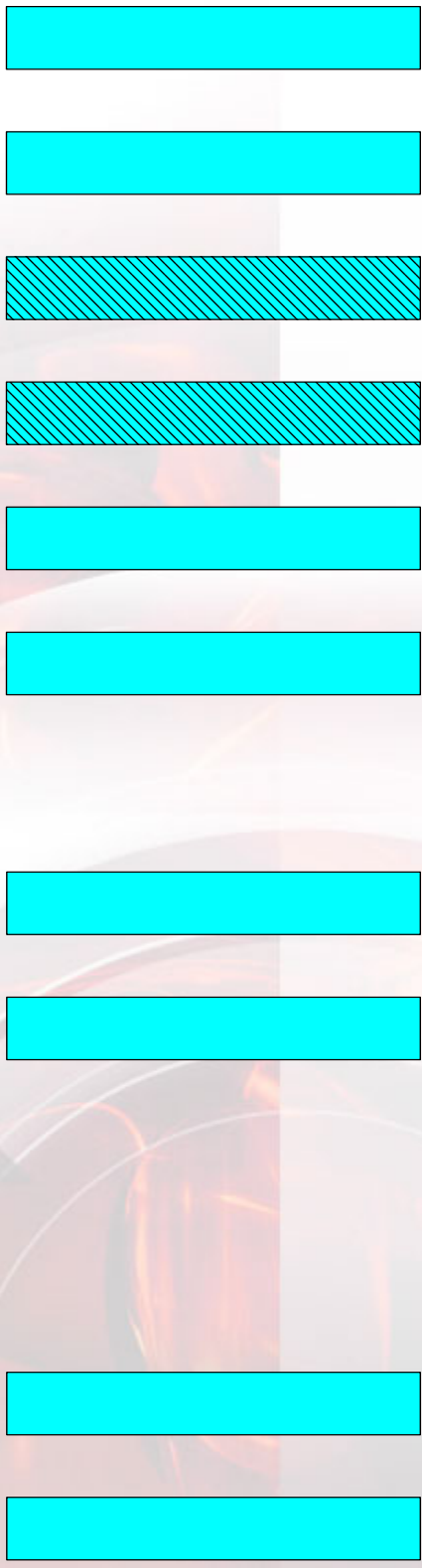
Design for Manufacture



- Minimum end-of-metal results in contact open
- Increase end-of-metal size to avoid the rounding effect



Design for Manufacture



- Non-uniform metal distribution, it affects the metal short and open
- Insert the dummy metal to maintain the uniformity across the chip



Chip/Package Integration

- Package Impact
 - Package model becomes more important for high speed interface design because simple package model is not sufficient to predict signal behavior
 - Thermal distribution is also highly dependent on the package. If the thermal gradient is large across the chip, it has negative impact toward the timing analysis

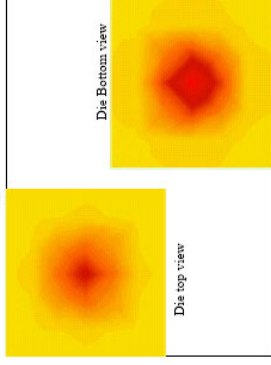


Chip/Package Integration

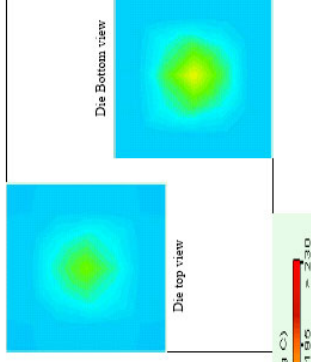
Power Consumption : 50W

HS Theta CA at 5C/W
Die temperature:
• Top : 229.7C
• Bottom : 233.4C
• Center : 229.7C
• Sides : 175.4C

Die 2D temperature view



HS Theta CA at 1C/W
Die temperature:
• Top : 151.1C
• Bottom : 153.5C
• Center : 151.1C
• Sides : 103.4C



- The temperature increase has direct impact toward the device/interconnect behaviors, it not limits to the chip itself but also affects other components
- The thermal gradient also introduces the timing difference between devices in various thermal regions within the chip.