

# Merging Traditional VLSI with Photonics

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Cornell University



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# Why Hybridize Optics to Electronics?

- Electrical interconnects designed to meet the interconnection requirements of future telecommunications and computing systems are costly and band limited.
- Short distance optical interconnects can provide benefits within high performance systems.
  - Power
  - Latency/data rates
  - Cost
- Multiple groups pursuing solutions:
  - Telecommunications equipment manufacturers
  - Computing systems manufacturers
  - Storage/disk farms
  - Auto Industry



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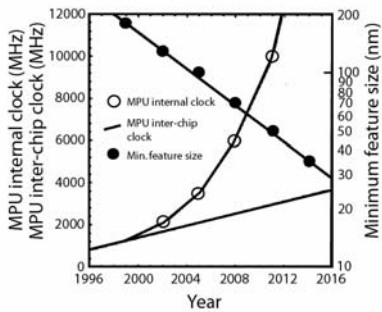
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# In Computer Systems .....

## Trend of MPU Clock Frequency



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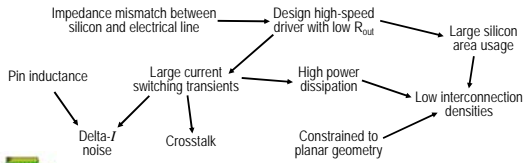
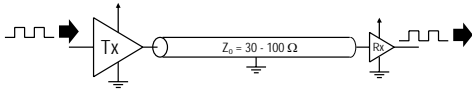
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## Electrical Lines have Low Impedance



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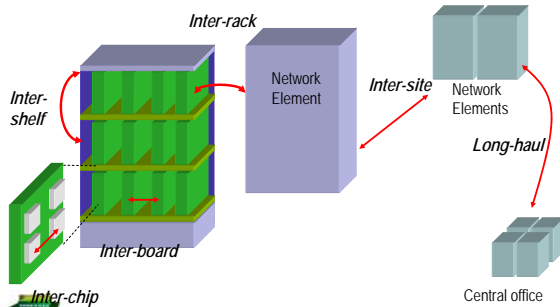
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## Opportunity for optical interconnect



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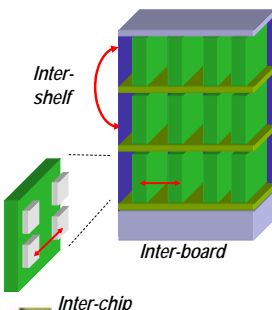
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## Optics "Inside the Box"



- Applies to:
  - Inter shelf/board/chip
- Optical interconnect options:
  - Serial & parallel fiber
  - Polymer waveguide
  - Free Space Optical Interconnects (FSOI)
- Enablers:
  - Transceivers
  - Optics
  - Packaging



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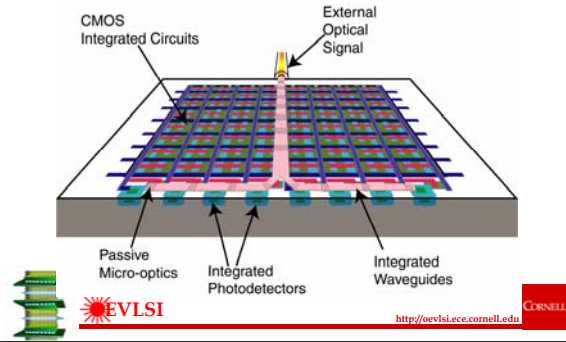
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## Bringing Optical Interconnects on Chip




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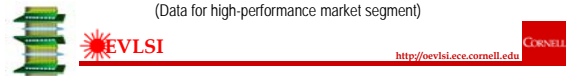
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## Application: Chip-to-Chip/ Board-to-Board

### International Technology Roadmap for Semiconductors

Year of Introduction	1999	2003	2005	2008	2011	2014
Technology node	180 nm	120 nm	100 nm	70 nm	50 nm	35 nm
Density (M/cm <sup>2</sup> )	24	78	142	350	863	2,130
Chip size (mm <sup>2</sup> )	450	567	662	713	817	937
On-chip clock (MHz)	1,250	2,490	3,500	6,000	10,000	13,500
Off-chip high-speed pins	700	1,500	1,900	2,300	2,700	3,000
Off-chip speed (MHz)	600	862	1,000	1,250	1,500	1,800

(Data for high-performance market segment)




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Off-chip high-speed pins	700	1,500	1,900	2,300	2,700	3,000
Off-chip speed (MHz)	600	862	1,000	1,250	1,500	1,800

'No known solution'




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## Cost of Electrical Interconnect

- Chip I/O: Cost per pin decreases, # of pins rises faster => need to decrease pin count to control cost
- Increasing demand for I/O BW:
  - Faster lines
  - Wider buses - costs of cable, area, expensive board material, limited pitch of lines
- Standard Practice: Cu on FR4 PCB
  - Insertion Loss @ 2 ft. 1GHz~10dB, 10GHz~50dB
- Other approach: Rogers 4000
  - BW extended by 2
  - Cost multiplied by 5
- Equalization: Complexity, area, still have to solve reflections and cross-talk

=> Escalating Costs for High Speed Interconnect Within the Box



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Optics can compete now, if we reduce cost.  
How do we reduce cost?

## Integration

A Monolithic Solution with a Low Number of Additional Processing/Packaging Steps is Best.



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## Transmitter Side Integration

Need to integrate:

- Sources
  - Hybridization
  - Optical Power Supply and modulators on chip
  - Silicon Sources
  - GaAs etc grown on Silicon
- Circuits
  - CMOS
  - BiCMOS
- Packaging
  - Waveguides
  - Fiber



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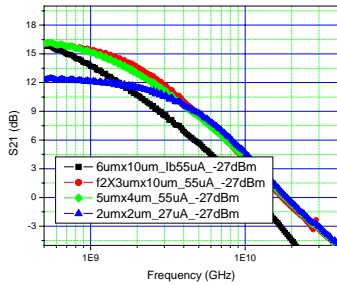
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## Photodetector Response Continued



-3dB bandwidth reaches 5GHz for the device with 2umx2um area.

Base biased with a current source to improve BW



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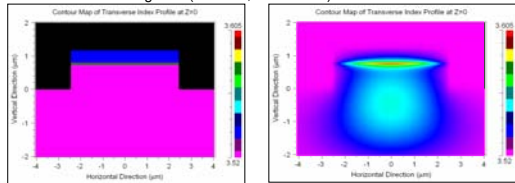
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## Lateral Coupling

Use Lateral coupling to increase effective length of the device and lengthen Path for absorption of lower energy photons  
Challenge: can we couple light laterally into such a thin region?

Optical Design and Simulation

- SiGe Internal Waveguide (15% Ge, 60nm thick) and Mode Simulation



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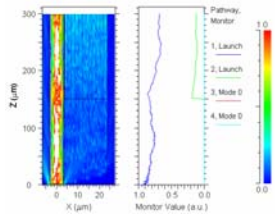
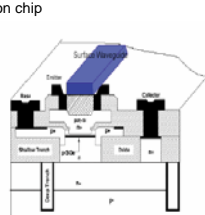
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## How Can We Get Light Into the Detector?

Polymer waveguide integration for evanescent coupling to SiGe region and optical signal routing on chip

18% power coupling from polymer waveguide to SiGe base layer.



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## Next Step, Monolithic Receivers

- We are currently working on the design and testing of the first fully monolithic Silicon Receivers ever published that is compatible with typical silicon electronics
- We have 2 versions of receivers in SiGe, optimized for low power consumption, so many can be integrated within a single chip.



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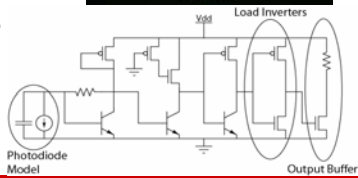
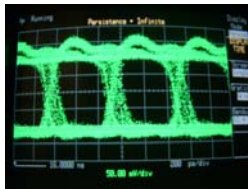
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## Receiver 1: Low power SiGe

- 2Gbps Bandwidth with BER $<10^{-13}$
- 250KW transimpedance
- 4.25mW power consumption
- Rail-to-Rail down to 10uA input current



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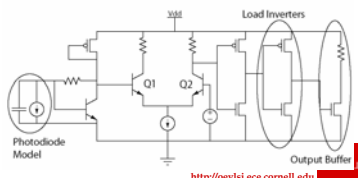
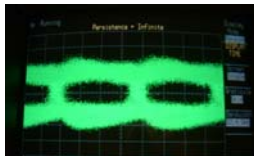
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## Receiver 2: Lower Power, Optimized for Latency

- 750Mbps Bit Rate
- 2.5mW Power consumption
- Transimpedance 25KOhm
- Tested with 10 uA input current
- Specific App.



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## Can Low Cost Optical Interconnect Have Benefits for On-Chip and Ultra-short Distances?



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## More Functionality?

- A. F. J. Levi [Proc. of the IEEE, 2000]  
 "Optical Interconnects in Systems"  
 o More functionality: e.g., optical switching, optical media access control.
- A. Pappu, A. Apsel [ISCAS, 2004]  
 "Electrical Isolation and Fan-out in Intra-Chip Optical Interconnects"  
 o Other Advantages: Electrical Isolation  
 o Link Length is not a parameter!



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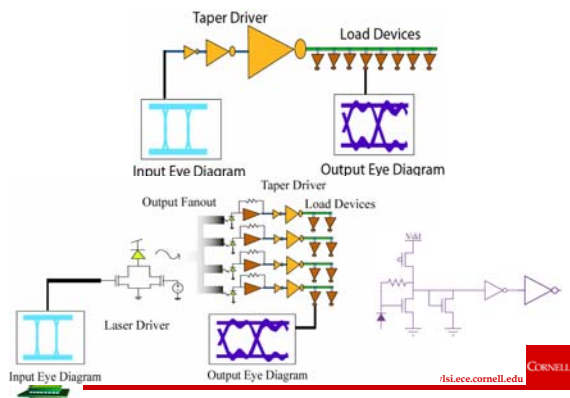
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## Electrical vs. Optical in Broadcast Architectures



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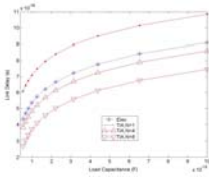
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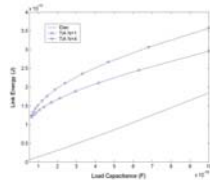
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### Some Results...



Link Delay vs Load Cap



Link Energy vs Load Cap



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### Some Results...

- Even for a small optical fan-out of four, we see improvement in delay.
- Relative increase in energy decreases as load becomes larger
- Energy delay product shows big improvement



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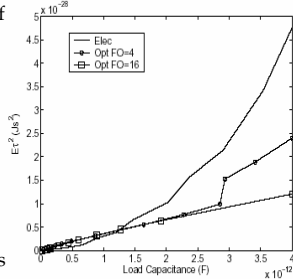
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### Adding Repeaters and Line length: Some Results...

- A small optical fanout of four is sufficient to breakeven with Electrical case.
- In 0.25 $\mu$ m technology, the load cap is 1.25pF corresponding to 250 min. sized inverters.
- Distances of 1.25mm and 450 $\mu$ m in 0.25 $\mu$ m and 0.09 $\mu$ m technologies resp.



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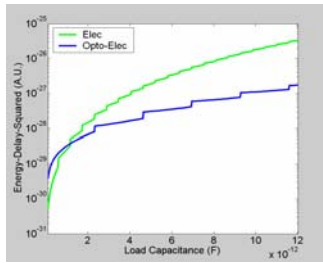
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## Et<sup>2</sup> Comparison



Adapted from "Analysis of Intra-Chip Electrical and Optical Fanout" Accepted Applied Optics



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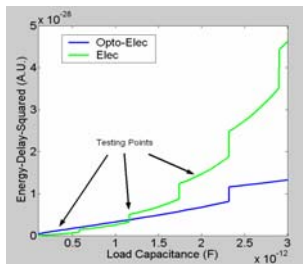
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## Testing Points



"Analysis of Intra-Chip Electrical and Optical Fanout" Accepted to Applied Optics



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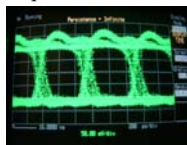
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## Some Results

- Fanout-of-Four Inverter Chain
- Average rise/fall delay 940ps
- Current Consumption at 1Gbps = 3.5mA
- BiCMOS TIA with Load Chain for optical fanout of eight.
- Average rise/fall delay = 600ps
- Current consumption at 2Gbps = 1.7mA



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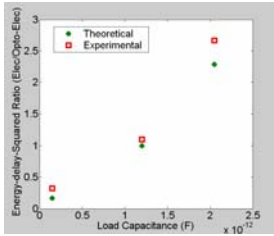
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## Comparison

- Testing results confirm theoretical predictions
- Graph shows opto-electronic system relative to electronic system performance

$$\frac{E\tau_{\text{Elec}}^2}{E\tau_{\text{Opto}}^2}$$



Adapted from Testing Results



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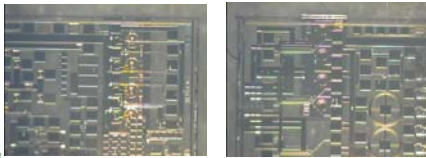
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## Other Receivers - SOS

- Silicon on Sapphire, SOS, what is it?
  - Flavor of SOI
  - Silicon is thin film grown on Sapphire
- Why use it?
  - High power efficiency at high speed
  - Transparent substrate



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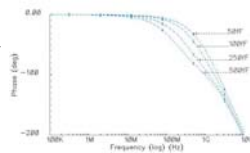
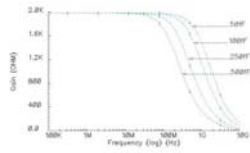
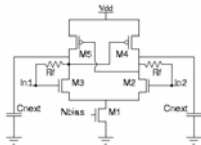
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## CMOS Optical Receiver in 0.5um



- Power consumption < 2.5mW
- >2.0 Gbps operation with 50fF photodetector
- 25 x 40 μm layout with gain stages

A. Apsel, Z. Fu, and A. Andreou. "A 2.5 milliwatt SOS CMOS Optical Receiver for Chip-to-Chip Interconnect", Journal of Lightwave Technology, Vol. 22, No. 9, Sept.2004.



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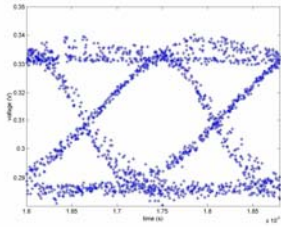
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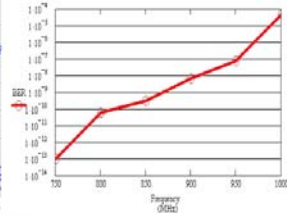
## Some Previous Results

Cin=250fF

BER @ 40uW



700 Mbps



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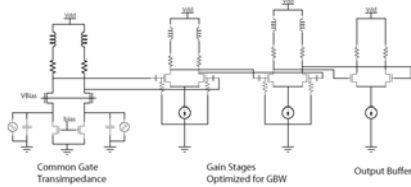
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## Next Generation SOS 10Gbps Receiver



- 0.25 um Process (no other 10Gbps in this process)
- 10 Gbps operation with BER < 10<sup>-12</sup>.
- Power < 100mW per channel



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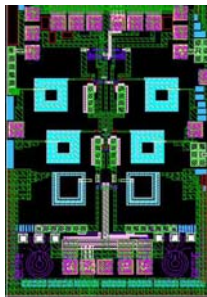
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## SOS 10Gbps Continued

- 0.25um SOS Technology
- Fully Differential Design
- Optimized number of stages to maximize gain-bandwidth product
- 7.5GHz Bandwidth (>10Gbps bit rate), 1.2KOhm impedance
- Low cost Datacom application



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## Conclusions

- Chip-to-chip OE interconnect in CMOS can replace wires for high speed interfaces
- Low cost integration in silicon is possible for both short and middle distance interconnect
- Even Intra-chip interconnect may have advantages that offer performance benefits for high-speed signaling
- Thanks to NSF and Lockheed-Martin for making this work possible
- Thanks to Anand Pappu, Tao Yin, Zhongtao Fu, Anthony Kopa



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